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CSAM: A clock skew-aware aging mitigation technique

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ABSTRACT

In this work, we propose a clock skew-aware aging mitigation (CSAM) technique which considers the effect of asymmetric aging both on logic path and clock tree together. Simultaneous consideration of both parts in the design optimization problem enables us to reduce the area overhead while increasing the lifetime. For the aging mitigation of the logic path, we make use of both internal node control (INC) and input vector control (IVC) techniques while, for the clock tree circuits, a proper choice between NAND or NOR based integrated clock gating (ICG) cell is made. The optimization may be performed based on two objective functions of maximizing lifetime or minimizing the area overhead for a predetermined clock frequency and lifetime. To assess the efficacy of the proposed technique, we compared the lifetimes and area overheads for a set of circuits from ISCAS89 and ITC99 benchmark suites when CSAM and conventional techniques are used. The results, obtained using SPICE simulations for the circuits in a 45-nm technology, reveals that an average lifetime improvement of 34% and an average area overhead reduction of 25.7% for the two objective functions, respectively.

1. Introduction

Bias Temperature Instability effects (BTI), Time Dependent Dielectric Breakdown (TDDB) and Hot Carrier Injection (HCI) are known as main sources of circuit aging and temporal performance degradation [1,2]. Among them, the BTI effect may be considered as a dominant reliability concern as the gate oxide becomes thinner especially in highly scaled technologies [3]. In the case of PMOS devices, the effect is induced due to a negative bias voltage, and hence, is called negative BTI (NBTI). The effect makes the threshold voltage more negative over time degrading the circuit performance and hence reduces the life time [4]. The results presented in [5–7] indicate that, in addition to the gate oxide thickness, the amount of NBTI-induced degradation exponentially depends on the operating temperature. In addition, the degradation is proportional to the amount of the negative bias voltage (stress). As the bias becomes more negative, the magnitude of the gate oxide field (E_{ox}) increases. Finally, the inversion layer hole density also plays an important role [5].

During the actual operation of the circuit, the bias voltage dynamically changes causing the PMOS device undergoing alternate stress and recovery periods (dynamic NBTI effect). In the stress condition, the magnitude of the threshold voltage increases due to the generation of interface traps at the Si-SiO_2 interface. During the recovery condition where the negative bias is removed, some of the interface traps are annihilated resulting in a partial recovery [4]. The recovery reduces the threshold voltage change (ΔV_T) for the AC (dynamic) stress compared to the case of the DC (static) stress where the threshold voltage shift is not reduced over the time. The amount of the threshold voltage shift recovery depends on the duty cycle and input patterns.

Conventional reliability analysis assumes either a DC stress condition or an average duty cycle if an AC stress condition is considered. Since during the actual operation, different parts of the circuit may have different operation modes (such as standby mode where clock gating may be invoked), even the AC stress condition with an average duty cycle cannot predict the impact of the NBTI effect with a sufficient accuracy [4,8]. During the standby mode, the input voltage of the PMOS device may have a LOW input voltage (corresponding to logic zero) where the transistor is under the static NBTI stress. Consequently, the standby mode leads to asymmetric degradation of the devices in all frozen parts of the circuit. This type of degradation is translated to more stress

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