Self-Impact of NBTI Effect on the Degradation Rate of Threshold Voltage in PMOS Transistors

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Abstract—reliability aware circuit design and estimation of circuit performance during lifetime is a critical challenge in design and test of integrated circuits in nanometer technology nodes. Negative Bias Temperature Instability (NBTI) as the most dominant aging source is deeply dependent on the operating temperature of the circuit. In this work, we have developed a simulation framework to dynamically estimate the effect of NBTI on power consumption of the circuit and consequently the operating temperature. The effect of NBTI on temperature will act as a natural negative feedback mechanism to reduce the degradation rate of threshold voltage ($V_{th}$). Simulation results show that estimated degradation in $V_{th}$ is about 4.1% less than the predicted amount by current models.

I. INTRODUCTION

Bias Temperature Instability effects (BTI), Time Dependent Dielectric Breakdown (TDDB) and Hot Carrier Injection (HCI) are known as main sources of circuit aging and temporal performance degradation [1]. As reported in [2] by IBM, Negative Bias Temperature Instability (NBTI) is the most severe degradation mechanism in the circuit lifetime domain as CMOS technologies scale beyond 90nm, and the impact of NBTI on circuit delay is about 15% on 65nm technology node. Thus studying the effects of NBTI on circuit lifetime will be the main focus of our work. The critical paths of the circuit may change in time according to the change caused by NBTI in threshold voltage of the PMOS transistors and consequently the delay of the circuit elements. So the reliability-aware design needs to consider gradual circuit performance degradation during lifetime to meet all needed performance metrics for the circuit without losing the overall functionality and violating the power/delay budget for circuit.

When PMOS transistors in circuits are under stress condition by negative gate voltage (i.e., $V_{gs} = -V_{dd}$) at elevated temperature, NBTI occurs causing a shift in threshold voltages [3], and resulting in the degradation of device performance. Biasing the PMOS gate at supply voltage ($V_{dd}$) in recovery condition, causes annealing of the majority of previous NBTI-induced degradation [3,4]. As illustrated in Fig. 1, because of the fast annealing rate at the beginning of recovery phase after stress, even a small recovery period (i.e. signal probability close to 1) greatly reduces the overall degradation by more than 50% of static stress [3].

When the PMOS transistor is under stress or recovery condition alternatively, the degradation of threshold voltage is partially recovered, which leads to less severe shifts over a long time compared to that under constant stress condition. Therefore, an accurate prediction of performance degradation should include not only the operating temperature of the circuit and its supply voltage, but also the switching activity of the node [3].

Several physical models has been introduced in recent researches to capture the effect of various factors such as temperature, oxide thickness, stress time (signal probability) and supply voltage on NBTI-induced degradation in threshold voltage of PMOS transistors [3-6]. Since NBTI is a thermally activated process, its aftereffects such as threshold voltage shift, current degradation and delay increment increase exponentially with the rise in temperature. However, the existing NBTI estimation approaches [3-6] have neglected the self-impact of this effect on threshold voltage degradation. Although the NBTI effect worsens the timing issues of the circuit, due to the exponential dependence of leakage power on threshold voltage, reduces the overall power consumption and as a result the average temperature of the die.