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A New Low-Power Architecture Design for Distributed Arithmetic Unit in FIR Filter Implementation

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Abstract In this article, an improved Distributed Arithmetic (DA) architecture is proposed, in which the high power consumed by adder units is relocated in the system to reduce the switching activity and total power needed. We used the concept of Time Domain Activity Duration Function (ADF) in architectural-level modification of target units at dynamic operating conditions. The proposed DA exploits the circuit activity, and the adder units are used in minimum states. The proposed DA is a run-time reconfigurable and lets system change the coefficients of FIR filter dynamically. The design was simulated, and the results were verified via two-phase power calculation method. The power calculations are based on forward synthesis invariant points and backward synthesis oriented activity approach. This method was applied to calculate the power and area of the proposed DA and other well-known counterparts in the literature. In the experimental results on 180 nm CMOS ASIC synthesis, the maximum clock of 100 MHz is achieved. In the 32-tap FIR filter implementation of our proposed DA and best known DA2 in serial DA structure, the switching power and internal power improvements are about 21 % and 10 %, respectively, in approximately equal speed and 5 % area increment.

Keywords Finite Impulse Response (FIR) filter · Multiply Accumulate (MAC) · Distributed Arithmetic (DA) · Activity Duration Function (ADF)

1 Introduction

Digital Signal Processing (DSP) algorithms are extensively utilized in signal conditioning by Field Programmable Gate Arrays (FPGA). Finite Impulse Response (FIR)

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