A Low-Power Low-Area Architecture Design for Distributed Arithmetic (DA) Unit

S. F. Ghamkhari, Shahed University
School of Engineering, Shahed University
Shahed University of Tehran
Tehran, Iran
ghamkhari@shahed.ac.ir

M. B. Ghaznavi-Ghoushchi, Shahed University
School of Engineering, Shahed University
Shahed University of Tehran
Tehran, Iran
ghaznavi@shahed.ac.ir

Abstract- In this paper an improved DA architecture is proposed. In the proposed DA, the high power consumption adder units are relocated in the system to lower the switching activity and total power. The proposed DA exploits the circuit activity and the adder units are only used just in minimum states. The designed DA is a run-time reconfigurable. The design is verified, and simulation results via 2-phase power calculations based on forward synthesis invariant approach and back ward synthesis oriented activity approach is used to calculate the power and area of the proposed DA and all known counterparts. In the experimental results on 180n CMOS ASIC synthesis the maximum clock of 180 MHz is achieved. In the 5-tape FIR filter implementation of our proposed DA with clock gating enabled and best known LUT Less2, the dynamic power and area improvements are 39.76% and 16.35% respectively.

Keywords- Multiply-Accumulator-Circuit (MAC); Distributed Arithmetic (DA); Finite-Impulse-Response (FIR) Filter.

I. Introduction

Digital Signal Processing algorithms are widely used in signal conditioning by conventional and high-end Field Programmable Gate Arrays (FPGA). Finite Impulse Response (FIR) filter is one of the major units in DSP. They are frequently used in image, video, audio and mixed media signals [1,2].

Multiply-Accumulator-Circuit (MAC) is the main core of FIR filter implementations [2,3]. It requires to use K-tapes in conventional MAC-based FIR design. This not only increases the design cost but also gains more design complexity [1,2,3,4]. To resolve the difficulties of MAC in FIR filters, the concept of DA was introduced by Croisier. It was based on 2's complement and a novel bit position reordering [1]. In DA the multiplier is interestingly removed which in turns reduces the final DA-based FIR area drastically over MAC-based FIR. DA-based FIR is also more suitable for low-power applications [2].

Generally, DA implementation is mainly in two ways of RAM-based and ROM-based methods. In ROM-based, all states are stored in the Look Up Table (LUT). This is technically called as pre-computation or pre-calculation and has a significant impact of low-power design. Therefore, ROM-based structures are highly efficient in power consumption and occupied area in the cost of fixed and pre-defined filter coefficients which in turn limits the application scopes. In another alternative approach, to implement the FIR filter, a RAM-based schema is used. In this case the fixed filter coefficients are stored as the contents of the RAM unit. This allows changing and modifying the filter coefficients during the run-time of the filter for different required applications. From the power and area efficiency, the power consumption and consumed chip area are more than the ROM-based methods. The low-power and compact size of the ROM-based approaches and higher degree of reconfiguration in RAM-based alternatives from one side and relatively higher power of the former and high power of the later from the another side, are the two major motivation factors for researchers attempting to reduce the gap between them.

The LUT model of ROM is used in DA, has an important role in filter performance; on the other hand whenever the filter size increases, the LUT or ROM complexity (area) of the implementation described in the DA architecture grows exponentially. Therefore, the reduction of LUT or ROM size is a one field of research in this subject.

Speed or operating clock frequency, power and area are three basic parameters in the FIR filter design and performance measures. This research is directed to propose power and area improved DA architecture. This achievement is also targeted with reconfigurable or

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