A High Performance, Race Eliminated, Two Phase Nonoverlapping Clocked All-N-Logic for both Strong and Subthreshold Designs

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Abstract: *In this paper, a new structure of ANL logic, named TPANL, is presented to achieve higher performance, lower power consumption and eliminating glitches. Different ANL logics suffer from output glitches due to race problem. Our proposed TPANL logic by two phase nonoverlapping clocks eliminates output glitches and reduces glitch power. TPANL logic speedup is mainly due to reduced capacitance at each evaluation node of a dynamic circuit. This logic works in both operational region of strong inversion and subthreshold region, with 10GHz to 12.5MHz respectively. In spite of NonInv./Inv. pipeline in ANL logics, TPANL is based on NonInv./NonInv. pipeline and therefore it solves the voltage drops on NMOS Inv. stages in subthreshold regions. The simulation results of 4-bit CLA adder show 27% and 72.9% power consumption reduction, also, 60% and 50% performance improvement, in strong inversion region rather than ANL and DPANL respectively. The 4-bit CLA adder with TPANL logic in the subthreshold region has about 92nW power consumption.*

Keywords: Dynamic circuits, All-N-Logic (ANL), low power, nonoverlapping clocks.

1. Introduction

High speed logic operation with low power consumption is a key component of microprocessors, super computers, telecommunication, and digital signal processing [1] [2] [3]. To achieve high speed logic operations, technologies such as Bipolar, GaAs, HEMT, and BiCMOS have the preference. Due to the problem of high cost, low packing density, and high power consumption, CMOS technology is preferred [1]. Therefore, design of high performance CMOS VLSI digital circuits, represents a great challenge. CMOS dynamic circuits have been widely used since they have faster switching speed and less area than the conventional static CMOS circuits [1] [3] [4]. Furthermore, to achieve higher throughput, pipelined structure has been used to increase the maximum operating frequency. Domino CMOS [5] only supports non-inverting logic. NO Race (NORA) [6] and Domino CMOS both have the charge redistribution problem. NORA logic uses two-phase clock signals instead of four-phase clock signals and eliminates the race problem [7]. The True Single Phase CMOS (TSPC) logic [8] uses a single-phase clock without inversion and due to avoid the clock skew problem, can operate at high clock frequency.

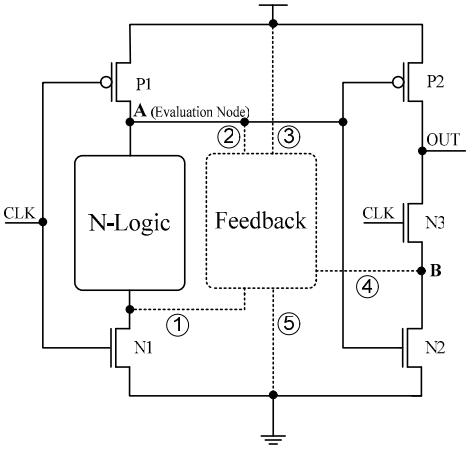

Fig. 1: Circuit diagram of ANL logic

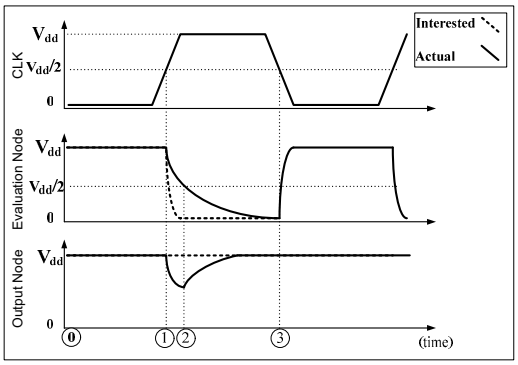

Fig. 2: Race problem in ANL logic

In pipelined systems with NORA, Zipper [9] [10], or TSPC structure NMOS and PMOS logic blocks are used and since PMOS logic blocks have low speed, they limit the performance of systems. In order to achieve higher speed, All-N-Logic (ANL) structure was introduced that removes limited speed of NORA, TSPC, and Zipper logics by using only high speed NMOS logic in all stages. ANL logic with its latch stage is widely used in pipelined systems.

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