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A 14.8 ps jitter low-power dual band all digital PLL with reconfigurable DCO and time-interlined multiplexers

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Abstract Using recently the developed dual band digitally controlled oscillator, in this paper, it can be proposed a low-power dual band all digital PLL (ADPLL). In the proposed ADPLL, toggling the input control bit utilizes the ADPLL to switch between two special frequency bands. An additional control circuit is also employed to have reasonable linearity. Sustaining coarse and fine characteristics and with a blend of capacitive shift and Schmitt trigger techniques, this oscillator changes the trigger points of the circuit and thus results in changeable delay and therefore, in creation of two different frequency bands. If the multiples of these bands used, it can cover two different frequency bands with one input toggling situation. It can be utilized in situation when it switched between two different frequencies for two unlike application or multi-standard bands. In such an occasion, instead of using two ADPLLs, the proposed structure, which decreases the needed area, can be used. Moreover, in this method, there is no need for redesigning and appraising the degree of stability against voltage changes, temperature and process of two ADPLLs. Simulation of the proposed dual band ADPLL is performed with Hspice by a voltage of VDD = 1.8v in 180 nm CMOS technology. The frequency range of the proposed dual band digitally controlled oscillator is from 97.18 to 117.65 MHz in lower band and 134.05–177.03 MHz in the high band.

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1 Introduction

Phase Locked Loop is a circuit for synchronizing frequency and phase of signals with a Ref. [1]. Due to the advantages of the digital design, including technology independency, higher noise margins, built-in rail-to-rail swing and ease of implementation with fewer layout and mismatch problems, compared to the analog one, there are reasonable demands on moving into all digital PLL circuits [1]. All-digital phase locked loop (ADPLL) is an effective example in this approach [1]. Generally, ADPLL is divided into two groups, one used in receivers for modulation and demodulation or changing channels or, etc. The other used for production and detection of data and time pulse as a frequency synthesizer. The main difference of the two groups is their oscillator design.

The main core of ADPLL is its digitally controlled oscillator (DCO) sub circuit that is responsible for power consumption and range of operating frequency. In DCO, the oscillation frequency is controlled by a vector bus of digital inputs. There are two types of DCO in conventional ADPLL designs [2]. They are either implemented by LC-tank circuits or ring oscillators (RO). The main design parameters in both are jitter, power consumption, operating frequency ranges, linearization and Process, supply voltage and temperature (PVT) tolerant. The LC-tank designs have best fine-tuned frequency resolutions using small but precise varactors. This implies very dense placement and higher complex lithography. Therefore, in the recent high resolution, DCO deigns the varactor is realized by NOR

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