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Low-noise differential transimpedance amplifier structure based on capacitor cross-coupled g_m-boosting scheme

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ABSTRACT

This paper presents a capacitor cross-coupled g_m-boosting scheme for differential implementation of common-gate transimpedance amplifier (CG-TIA). A differential transimpedance amplifiers (DTIA) is designed by this scheme using two modified floating-biased CG stage with improved low corner frequency. Despite conventional methods for single-ended to differential conversion that increase the power and the noise for the same gain, the new DTIA gives a higher gain and hence reduces the input-referred noise power. Design of the DTIA circuit using 0.13 μm CMOS technology illustrates near 1.7 dB improvement in the circuit sensitivity and 5.2 dB enhancement in transimpedance gain compared to its single-ended counterpart. Operation at very low frequencies and stable dc coupling to photodiode are other features of the proposed DTIA.

1. Introduction

In optical receivers, transimpedance amplifiers (TIA) are the most critical and noise-sensitive elements [1], as they act as the interface between the electronics and the optics. Compared to TIA with single-ended configuration, differential TIA is generally preferred because of providing better immunity to power supply and substrate noises. However, photodiodes (PD) produce a single-ended current and single-ended to differential conversion (SDC) methods generally increase power consumption, and degrade the noise performance [1,2].

In this paper, we develop a new method to obtain SDC in common-gate transimpedance amplifier (CG-TIA) by means of g_m-boosting principle. Theoretical foundations for gain, bandwidth and noise analysis are developed.

Rest of the paper is organized as follows. Section 2 summarizes the conventional SDC design methods. Section 3 describes the effectiveness of g_m-boosting technique for SDC design. Section 4 presents a new differential TIA structure and the circuit realization. In Section 5, we present the simulation results followed by discussions. Section 6 is dedicated concluding remarks. The paper includes three Appendices. Appendix A is devoted to noise analysis of the CG-TIA, while Appendices B and C cover the detailed analysis of transimpedance gain and noise of the differential TIA (DTIA), respectively.

2. Conventional SDC methods

A common approach for SDC in TIA circuits is using a differential pair at the output, which is implemented in three methods as described below. In the first method, a replica (dummy) circuit of the single-ended TIA can be integrated with the main one so as a differential signal would appear at the output [1,3], as shown in Fig. 1(a). This architecture suffers from several nonidealities: (i) the paths from input to the outputs of main and dummy TIA are not the same, leading to gain and phase discrepancy at the output, especially for high-frequency components of the signal [2]; (ii) the output signals are not fully differential and there would be an inherent dc offset (about half the output signal swing) between them, causing serious problems in choosing a decision threshold; (iii) if the circuit is dc coupled to the PD, the main TIA experiences photocurrent dc-level fluctuations, leading to instability in its dc-bias conditions which affects the dummy circuit too; (iv) a gain equal to that of single-ended one is achieved while the power consumption is doubled; and (v) the input-referred noise current of the circuit is $\sqrt{2}$ times that of single-ended one, degrading the sensitivity by 3 dB [1,2].

Fig. 1(b) depicts the second method for converting the output of a single-ended TIA to a differential signal. In this method, we extract the dc component of the output signal of the TIA by a

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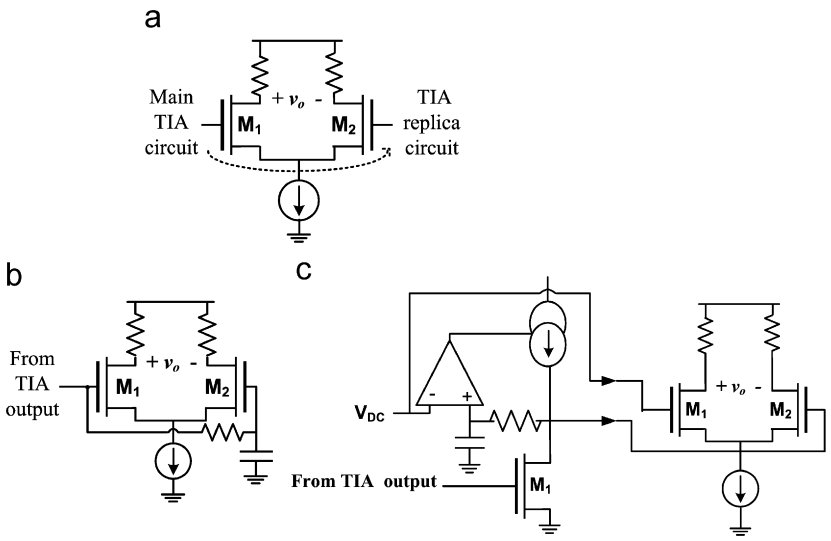

Fig. 1. Providing single-ended to differential conversion: (a) using a replica circuit; (b) extracting dc content of TIA output and applying the result to a differential pair and (c) auto-dc-control circuit.

RC low-pass filter. Then, this component is used along with the signal to feed the inputs of a differential pair. The output signal of the differential pair is free from offset. However, the filter requires a relatively large external capacitor due to its large time constant [2,4]. In addition, the variations in dc component of single-ended TIA output will leak to the differential output and may affects overall differential characteristics.

Fig. 1(c) illustrates the third method for SDC design. It uses an auto-dc-control circuit [5] to force the dc-output level of TIA to a fixed value, usually equal to the common mode voltage needed for subsequent circuitry. The output of the TIA and the dc-level drive a differential pair at the front-end of a limiting amplifier. The circuit complexity that offers extra power consumption is associated with this technique.

3. G_m-Boosting technique for SDC

The conventional CG configuration of TIA (CG-TIA) is shown in Fig. 2, where C_{in} includes PD parasitic capacitance and gate–source and source–bulk capacitances of the transistor and C_{out} contains the input capacitance of the following stage plus gate–drain and drain–bulk capacitances. The transimpedance gain can be written as

$$Z_T = \frac{g_m + g_{mb}}{g_m + g_{mb} + 1/R_S} \frac{R_D}{(1 + S/\omega_{p,in})(1 + S/\omega_{p,out})} \quad (1)$$

where $\omega_{p,in} = (g_m + g_{mb} + 1/R_S)/C_{in}$ and $\omega_{p,out} = 1/(R_D C_{out})$ denote the input and output poles.

Neglecting channel-length modulation, input-referred noise current spectral density of the CG-TIA, as shown in (A.8), is approximately given by

$$\overline{i_{n,in}^2} \cong \frac{4kT}{R_S} + \frac{4kT}{R_D} + \frac{4kT(\gamma g_m + 1/R_D)}{(g_m + g_{mb})^2}(\omega^2 C_{in}^2 + 1/R_S^2) \quad (2)$$

where k is Boltzmann's constant, T is the absolute temperature and γ is the noise factor of the MOSFET.

By using g_m-boosting technique [6–9], illustrated in Fig. 3(a), the effective transconductance of the transistor is increased to $G_{m,eff} = (1+A)g_m$, where A is the gain of the inverting amplifier connecting the source to gate. Note that g_m-boosted common-gate-low-noise amplifier (CG-LNA) exhibits lower noise figure than conventional CG-LNA. For instance, assuming an inverting amplifier without significant noise [7], the noise factor of g_m-boosted CG-LNA is $F = 1+\gamma/[\alpha(A+1)]$, while the noise factor of a conventional CG-LNA is $F = 1+\gamma/\alpha$, where $\alpha = g_m/g_{d0}$ [8].

Principle of a g_m-boosted CG-TIA is illuminated in Fig. 3(b). To identify how the g_m-boosting technique affects the system performance, consider transimpedance gain of the circuit

$$Z_T = \frac{G_{m,eff} + g_{mb}}{G_{m,eff} + g_{mb} + 1/R_S} \frac{R_D}{(1 + S/\omega_{p,in})(1 + S/\omega_{p,out})} \quad (3)$$

where $\omega_{p,in} = [G_{m,eff} + g_{mb} + 1/R_S]/C_{in}$ and $\omega_{p,out} = 1/(R_D C_{out})$. Comparing (3) with Z_T of a conventional CG-TIA, as given in (1), improvements in the dc gain and frequency response is apparent. For small values of R_S there is a considerable improvement in dc gain, while for large values of R_S, the improvement in frequency response would be more significant (considering that $\omega_{p,in}$ is usually dominant pole).

Assuming the inverting amplification stage in Fig. 3(b) does not contribute significant noise and neglecting channel-length modulation, input-referred noise current spectral density of the circuit is

$$\overline{i_{n,in}^2} \cong \frac{4kT}{R_S} + \frac{4kT}{R_D} + \frac{4kT(\gamma g_m + 1/R_D)}{(G_{m,eff} + g_{mb})^2}(\omega^2 C_{in}^2 + 1/R_S^2) \quad (4)$$

It is evident from (4) that the noise contributed by M_1 and R_D to the input is reduced in g_m-boosted CG-TIA.

Implementing inverting amplifier in Fig. 3(a) as an active stage may introduce several design issues due to its noise contribution and power consumption. On the other hand, differential implementation of the g_m-boosting technique, as illustrated in Fig. 4(a), enables using positive gain stages, of course when input is a differential signal. Thus, it will be possible to utilize passive elements, such as capacitors for the specific case of $|A| \approx 1$, as the gain stage [6–8].

Even though, differential implementation of g_m-boosting technique usually is applied when input signal is also available in differential form, we will demonstrate that it is possible to utilize differential g_m-boosting technique in situations where input signal is in the single-ended form. Fig. 4(b) illustrates this idea, by a basic configuration of differential g_m-boosting technique as capacitor cross-coupling of two CG-TIA. Assuming C_c in Fig. 4(b) is sufficiently large compared to parasitic capacitances, $v_{gs1} = -v_{gs2}$ where v_{gs1} and v_{gs2} represent the gate–source voltages of M_1 and M_2, respectively. Therefore, neglecting the

body effect and channel-length modulation, the drain current of M_1 and M_2 are related by $i_{d1} = -i_{d2}$. By assuming equal drain load, both the gain and the output noise per unit bandwidth are doubled compared to the conventional CG-TIA. As a result, the input-referred noise is reduced by $\sqrt{2}$, improving the circuit sensitivity by 3 dB. Note that in practice, this improvement may be lower because of the above-mentioned second-order effects. Furthermore, one should note that, the differential structure required for implementing the capacitor cross-coupling technique would not contribute to gain improvement since the input is single ended. Therefore, the above improvement is due to capacitor cross-coupling technique.

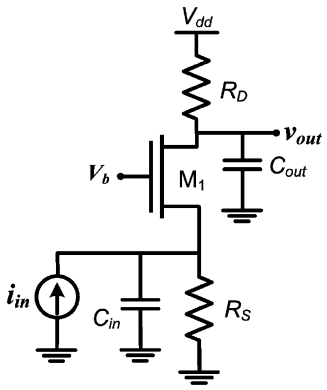

Fig. 2. Conventional CG-TIA.

In optical receivers, dc coupling to PD is preferred to achieve near dc-extended frequency response. However, dc coupling deteriorates the whole system performance stability, since changing average optical power level at the input will change the dc level of produced photocurrent, significantly altering the dc-bias conditions of the circuit [10]. In Fig. 4(b), the left part of the circuit directly couples to the PD and faces such a problem. Hence, the dc level of signals at the output of the left part becomes unstable depending on the received optical signal, while the output of the right part remains unaffected. This problem causes many design issues for subsequent stages. A solution to this problem is floating biasing of CG-TIAs as shown in Fig. 5(a), where the dc-bias currents through M_1 is held constant by forming a floating current mirror with M_0, as described in [10]. In other words, dc part of the i_{in} will be grounded through R_s, while its ac part will be directed toward R_d of course when the gate of M_1 can be considered ac grounded by C_B [10,11]. Fig. 5(b) exhibits the

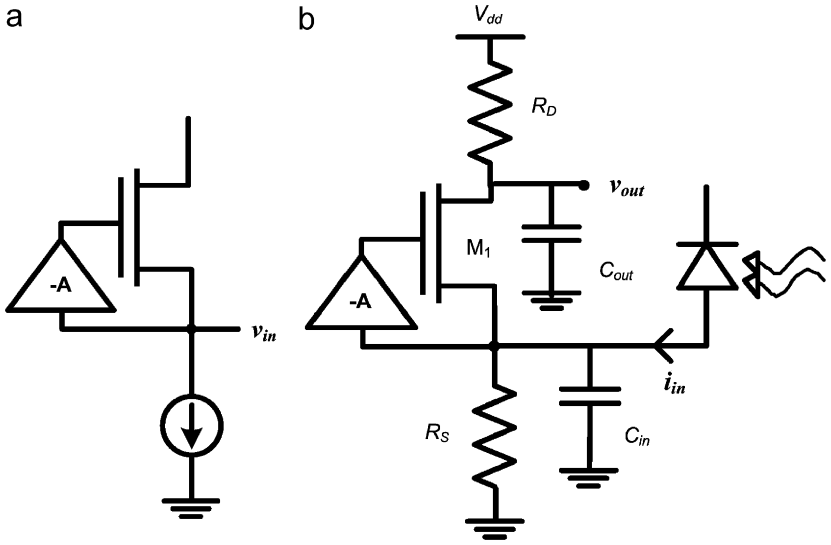

Fig. 3. G_m-boosting scheme: (a) principle, (b) topology of g_m-boosted CG-TIA.

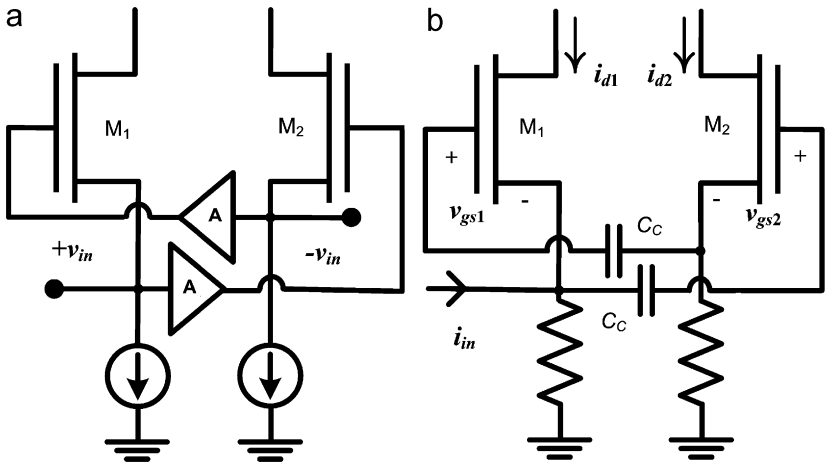

Fig. 4. (a) Differential implementation of g_m-boosting technique, (b) SDC by means of g_m-boosting technique.

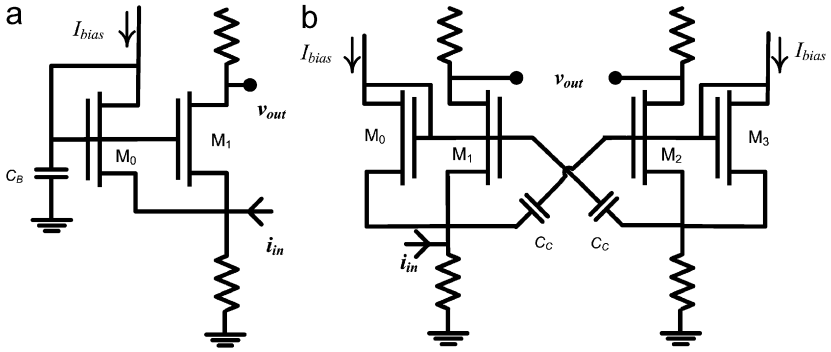

Fig. 5. (a) Floating-biased CG-TIA, (b) G_m-boosted differential CGTIA with its biasing circuitry.

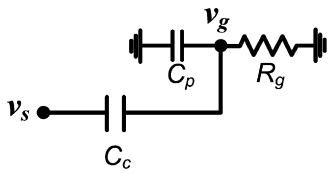

Fig. 6. Equivalent circuit for coupling by C_c.

proposed differential TIA with its biasing circuitry. In this circuit, the cross-coupling capacitors also work as gate bypassing capacitor for floating biasing.

4. G_m-boosted differential TIA (DTIA)

Three factors affect the coupling efficiency in the circuit of Fig. 5(b): parasitic capacitors at the gates, C_p; the impedance of gate biasing circuitry, R_g; and the frequency of incoming signal, i_{in}; as shown in Fig. 6 as an equivalent circuit for coupling mechanism by C_c. The inverting amplification value, A, in Fig. 5(b) is approximately given by

$$A = \frac{v_g}{v_s} = \left(1 + \frac{C_p}{C_c} + \frac{1}{R_g C_c S}\right)^{-1} \tag{5}$$

In order to have C_c working as a unity gain stage, the conditions $C_c \gg C_p$ and $\omega \gg 1/R_g C_c$ must be satisfied.

A wideband frequency response with a low cut-off frequency as close to dc as possible is needed for TIA circuits to operate free from *baseline wander* and *intersymbol interference* (ISI), and also to relax data coding requirement [10]. To achieve this by the architecture of Fig. 5(b) where coupling of signals takes place just for frequencies beyond $1/R_g C_c$, we need a large R_g. Called modified floating biasing, in Fig. 7(a) the resistor R_B is placed in series with gate to increase gate-biasing impedance [12]. In Fig. 7(b), R_B is implemented using a MOS transistor operating in subthreshold region [13].

Fig. 8 shows the modified version of the circuit of Fig. 5(b), obtained by capacitor cross-coupling of two modified floating-biased CG pairs. Although the floating biasing is only required for the left pair, it is used for the right pair to simply match the characteristics of the pairs.

Assuming $g_{m1} = g_{m2} = g_m$ and $g_{mb1} = g_{mb2} = g_{mb}$, and neglecting channel-length modulation, the drain current for M_1 and M_2 (i_{d1} and i_{d2}) can be obtained similar to (B.2) and (B.5), respectively:

$$\frac{i_{d1}}{i_{in}} = \frac{-R_{S1}}{1 + (g_m + g_{mb})R_{S1}} \frac{g_m + g_{mb} + 2g_m g_{mb} R_{S2} + g_{mb}^2 R_{S2}}{1 + (g_m + g_{mb})R_{S2}} \tag{6}$$

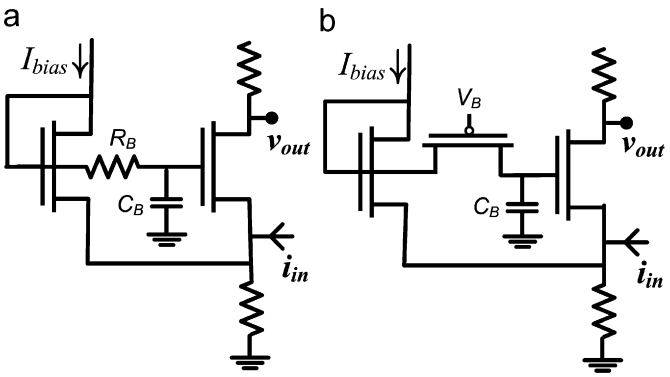

Fig. 7. (a) Modified floating-biased CGTIA, (b) implementing RB by a MOS transistor operating in subthreshold region.

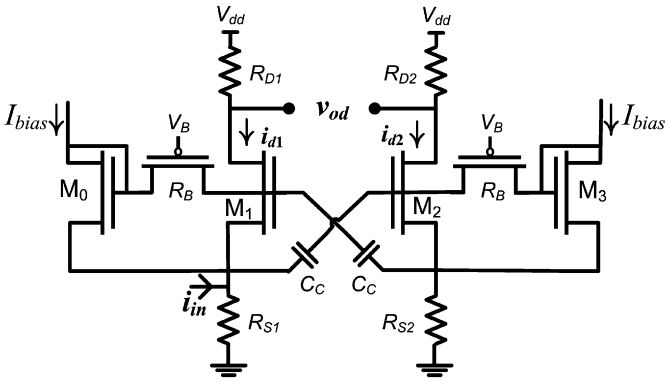

Fig. 8. Single-ended to differential g_m-boosted CG-TIA (DTIA).

$$\frac{i_{d2}}{i_{in}} = \frac{R_{S1}}{1 + (g_m + g_{mb})R_{S1}} \frac{g_m}{1 + (g_m + g_{mb})R_{S2}} \tag{7}$$

where i_{in} is the photocurrent. Dividing (6) by (7) yields

$$i_{d1} = -\left[1 + 2g_{mb}R_{S2} + \frac{g_{mb}}{g_m}(1 + g_{mb}R_{S2})\right] i_{d2} \tag{8}$$

This relation reveals that the value of i_{d2} is less than the value of i_{d1}. When the body effects in M_1 and M_2 are suppressed, $g_{mb} = 0$ and $i_{d1} = -i_{d2}$. However, this may bring some technological limitations in an n-well technology since the transistors should be placed in a p-well. An alternative way is to minimize R_{S2} in (8) as follows.

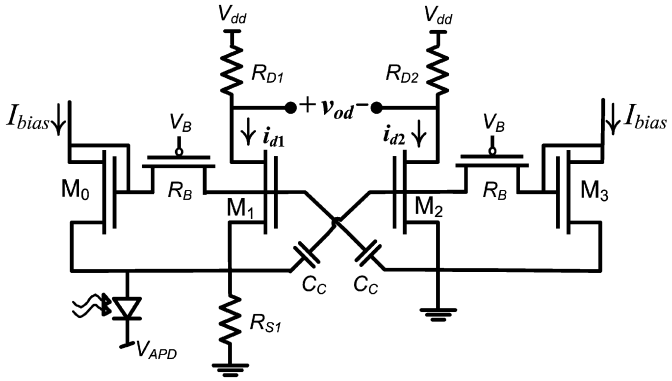

Fig. 9. Omitting R_{S2} in g_m-boosted DTIA to achieve higher differential gain.

Assuming $R_{D1} = R_{D2} = R_D$, the differential gain of the circuit, as shown in (B.8), becomes

$$Z_{T_0}|_{DTIA} = \frac{g_{m2}(1+g_{mb1}R_{S2}) + (g_{m1}+g_{mb1})(1+g_{mb2}R_{S2})}{(1+(g_{m1}+g_{mb1})R_{S1})(1+(g_{m2}+g_{mb2})R_{S2})} R_{S1}R_D \quad (9)$$

Ratio of the transimpedance gain of a DTIA to a conventional CG-TIA, is given by (B.10)

$$\frac{Z_{T_0}|_{DTIA}}{Z_{T_0}|_{CG-TIA}} = \frac{1+g_{mb2}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}} + \frac{g_{m2}}{g_{m1}+g_{mb1}} \frac{1+g_{mb1}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}} \quad (10)$$

According to (1) and (8)–(10), when $R_{S2} = 0$ and $g_{m1} = g_{m2} = g_m$, we have

$$\begin{cases} i_{d1} = -\left(1+\dfrac{g_{mb}}{g_m}\right) i_{d2} \\ Z_{T_0}|_{DTIA} = \left(1+\dfrac{g_m}{g_m+g_{mb}}\right) Z_{T_0}|_{CG-TIA} = \dfrac{2g_m+g_{mb}}{g_m+g_{mb}+1/R_S} R_D \end{cases} \quad (11)$$

Eq. (11) reveals that, eliminating R_{S2} is sufficient for obtaining a nearly doubled differential gain and the difference between the drain currents is small. Note that eliminating R_{S2} will result in negligible dc imbalance at the output due to biasing with current mirror.

Fig. 9 illustrates the circuit of Fig. 8 for $R_{S2} = 0$, where M_2 has a common-source configuration. The input-referred noise current spectral density of the circuit, as shown in (C.11), is approximated by

$$\overline{i_{n,in}^2} \cong 4kT\left\{R_S^{-1} + \gamma g_m \frac{(\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m+g_{mb})^2}\left[\left(\frac{g_m}{g_m+g_{mb}}\right)^2 + 1\right] + \frac{(g_m+g_{mb})^2 + (\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m+g_{mb})^2} \times \left\{\left[\left(\frac{g_m}{g_m+g_{mb}}\right)^2 + 2\right] R_D^{-1} + \gamma g_m\right\}\right\} \quad (12)$$

In deriving this equation the noise contributions of M_0 and M_3 are neglected, since they have smaller dimensions compared to the M_1 and M_2 [10]. In addition, the total current noise per unit bandwidth generated by a subthreshold MOS transistor is proportional to its current [14]. Since this is small in transistors implementing R_B, the noise contribution of these transistors can be neglected.

5. Simulation results

The circuits in Figs. 2 and 9 are simulated with Hspice(RF) in a 130 nm CMOS process, with threshold voltage of 0.326 and −0.324 V for nMOS and pMOS, respectively. The circuit parameters for simulation are given in Table 1. The performance plots for typical process parameters are shown in Figs. 10–14. A PD capacitance of 300 fF and a bondwire inductance of 500 pH have

Table 1
Circuit parameters

Parameter	Value	Unit
$(W/L)_{1,2}$	10/0.13	μm/μm
$(W/L)_{0,3}$	1.3/0.13	μm/μm
$(W/L)_{RB}$	0.26/1.3	μm/μm
R_B	2	MΩ
$R_{D1,2}$	400	Ω
$R_{S1,2}$	100	Ω
C_C	1	pF
V_{dd}	1.2	V
V_{TN}	0.326	V
V_{TP}	−0.324	V
V_b	0.4	V

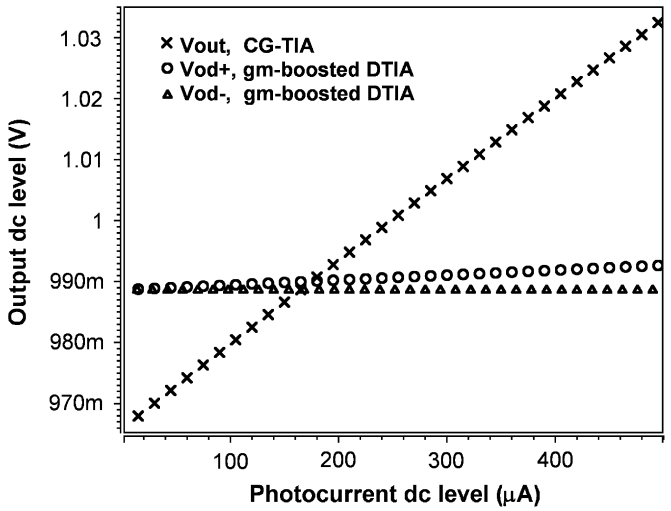

Fig. 10. Dependency of the outputs dc levels to the dc content of the input photocurrent.

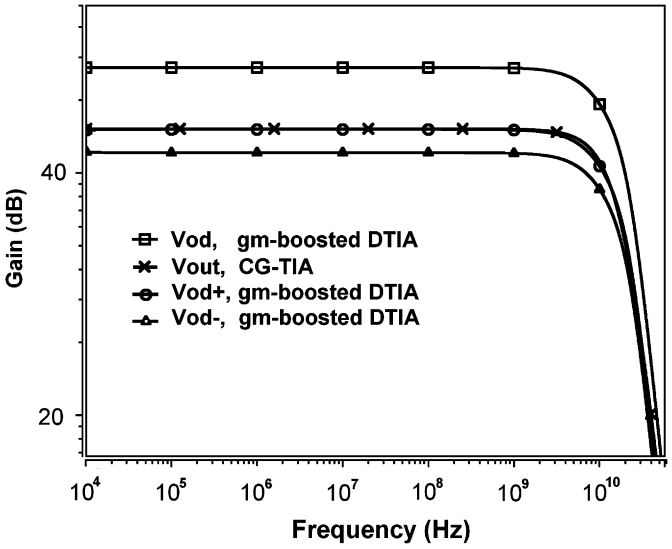

Fig. 11. Frequency response of CG-TIA and DTIA.

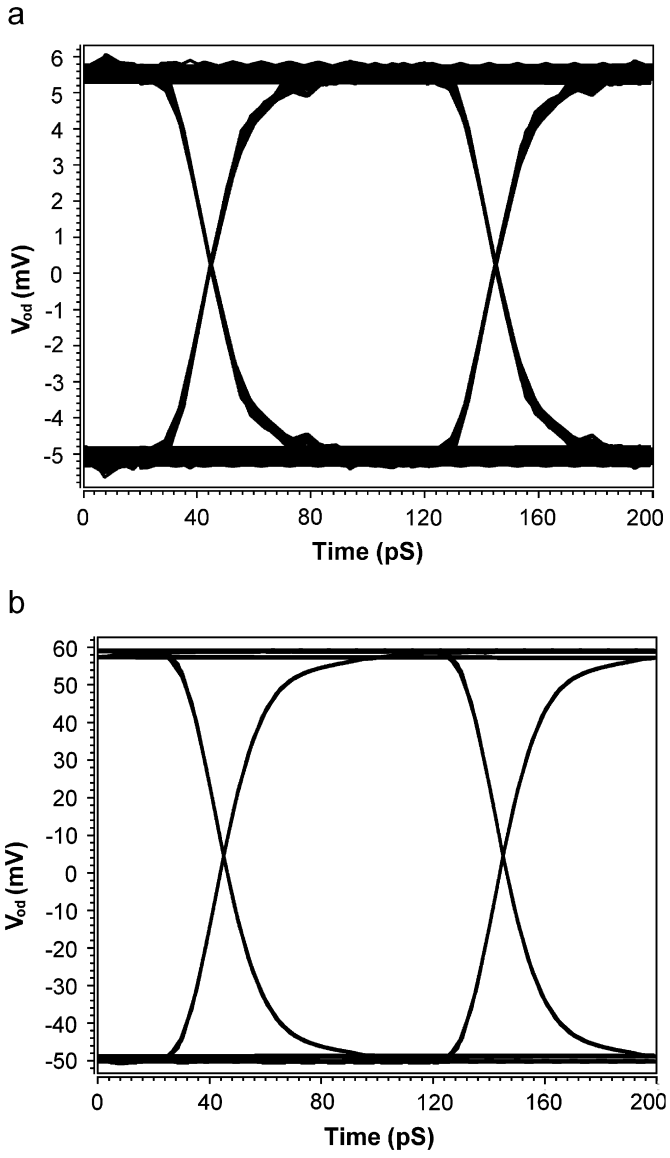

Fig. 12. Transient response to a 10 Gb/s random bit pattern: (a) $P_{in} = P_1 - P_0 =$ 10–50 μA, (b) $P_{in} = P_1 - P_0 =$ 100–500 μA.

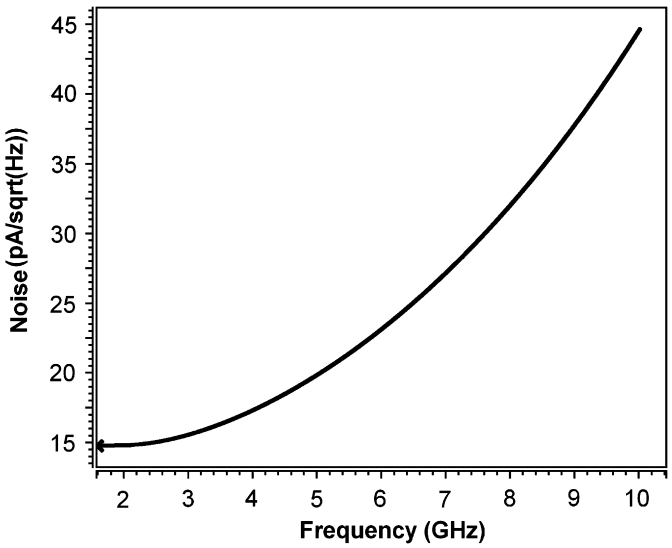

Fig. 13. Noise-current spectral density of CG-TIA and DTIA.

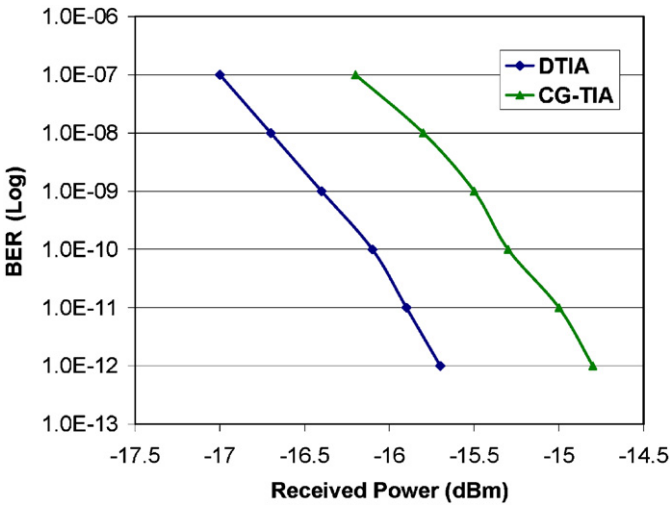

Fig. 14. 10-Gb/s BER performance of CG-TIA and DTIA.

been used for all simulations. Fig. 10 shows the dependency of the outputs dc levels to the dc content of the input photocurrent for CG-TIA and DTIA. While V_{od-} remains unaffected, the slope of V_{od+} is about one-eleventh comparing to the slope of v_{out} in CG-TIA in response to a 0–500 μA variation in input dc level.

Fig. 11 shows the frequency response of the circuits for $C_C = 1$ pF. The value of C_p is about 40 fF. The differential gain is 48.9 dB Ω, which is boosted by a factor of 1.82. The transimpedance gain for the left pair is 43.7 dB Ω, which is equal to that of the CG-TIA, while for the right pair is 42.1 dB Ω. A −3 dB frequency of 10.04 and 10.12 GHz can be seen for DTIA and CG-TIA, respectively. Although one of the cross-coupling capacitors is directly connected to the input node, the high-frequency corner is slightly deteriorated, since an extremely high-value resistor follows this capacitor. Further, the parasitic capacitors add a negligible extra capacitive load to the input node.

The transient simulations for a 10-GB/s random bit pattern in Fig. 12 reveal a completely open eye for two different-level inputs with extinction ratio of $r_e = 5$. The input average current level is approximately 30 and 300 μA for Fig. 12(a) and (b), respectively. A small dc difference at differential outputs can be seen in the transient responses, which are due to both the dc content of input current and the drain current mismatches of M_1 and M_2.

The noise current spectral density of the DTIA is shown in Fig. 13. It is observed that the noise current spectral density slowly increases at high frequencies. According to (12), at high frequencies ωC_{in} increases, thus the noise contribution of M_1 and M_2 and load resistors, R_D, to the input will increase. Fig. 14 demonstrates the BER graphs of the CG-TIA and DTIA. The optical sensitivity for CG-TIA and DTIA is obtained as −14.8 and −15.7 dBm W, respectively, using a PD responsivity of $\rho = 0.9$ A/W for a BER of 10^{-12} from following relation [15]:

$$P_{ave}(\text{dBm}) = 10\log\left(\frac{\overline{i_n}\,\text{SNR}}{2\rho}\frac{r_e+1}{r_e-1}\times 1000\right) \quad (13)$$

One should note that it is possible to achieve a better gain and noise performance in expense of a high-power consumption. However, the sensitivity of −15.7 dBm W is sufficient for short haul applications, which requires −12 dBm, according to SONET OC192 standard. The DTIA is employed in a 10-Gb/s optical receiver with limiting amplifier (LA) and clock-recovery circuit.

Table 2
Performance comparison of recent CMOS TIAs for 10-Gb/s operation

Specification	Ref. [16]	Ref. [11]	Ref. [17]	This work	
				(CG-TIA)	(DTIA)
Technology (nm)	120	250	180	130	130
Power consumption (mW)	3	1.6	34	0.69	1.4
Transimpedance gain	50 dB Ω Differential	42.2 dB Ω Single-ended	52 dB Ω Single-ended	43.7 dB Ω Single-ended	48.9 dB Ω Differential
Bandwidth	N/A	N/A	7.5 GHz	10.12 GHz	10.04 GHz
Photodiode parasitic capacitance	N/A	N/A	250 fF	300 fF	300 fF
RMS input noise	N/A	N/A	N/A	2.8 μArms	2.3 μArms
Optical sensitivity for BER = 10^{-12} (dBm W)	−13.1	−13.6	−19	−14.8	−15.7

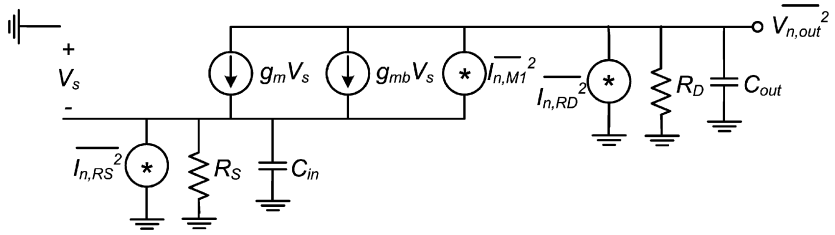

Fig. A1. High-frequency noise model of CG-TIA.

The optical sensitivity of the TIA followed by LA was reduced to −14.1 dBm W.

The performance parameters of CG-TIA and DTIA along with other recently published TIA data are given in Table 2. The power dissipation of DTIA is twice than that of CG-TIA, while its input referred noise current is reduced by a factor of 0.82, which illustrates 1.7 dB improvement in the circuit sensitivity.

6. Conclusions

The capacitor cross-coupled g_m-boosted differential TIA is implemented using two modified floating-biased CG stage. This novel approach can advantageously replace other differential design methods regarding to its simplicity, higher gain and better sensitivity. Simulation results with HSpice(RF) show that, despite the conventional methods for SDC that doubles the power and the noise for the same gain, the new DTIA gives a higher gain and hence reduces the input-referred noise power. Design of the DTIA circuit using 0.13 μm CMOS technology illustrates near 1.7 dB improvement in the circuit sensitivity and 5.2 dB enhancement in transimpedance gain compared to its single-ended counterpart.

Acknowledgement

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Appendix A. Noise analysis of the CG-TIA

Fig. A1 shows the high-frequency small-signal noise model of CG-TIA. Since the noise current of R_S, denoted by $I_{n,RS}$, is directly added to the input, it is ignored in the analysis and finally will be added to the results. Neglecting channel-length modulation, we have

$$-V_S = (I_{n,M1} + g_m V_S + g_{mb} V_S)(C_{in} S + 1/R_S)^{-1} \quad (A.1)$$

$$-V_S = [-V_{n,out}(C_{out} S + 1/R_D) + I_{n,RD}](C_{in} S + 1/R_S)^{-1} \quad (A.2)$$

From (A.1) and (A.2), we have

$$V_{n,out} = \frac{I_{n,RD}}{C_{out} S + 1/R_D} + \frac{(C_{in} S + 1/R_S) I_{n,M1}}{(g_m + g_{mb} + C_{in} S + 1/R_S)(C_{out} S + 1/R_D)} \quad (A.3)$$

The transimpedance gain of the CG-TIA given in (1) can be rewritten as

$$T_Z = \frac{(g_m + g_{mb})}{(g_m + g_{mb} + C_{in} S + 1/R_S)(C_{out} S + 1/R_D)} \quad (A.4)$$

Dividing (A.3) by (A.4) yields

$$I_{n,in} = \frac{C_{in} S + 1/R_S}{g_m + g_{mb}} (I_{n,M_1} + I_{n,R_D}) + I_{n,R_D} \quad (A.5)$$

By adding the noise of R_S to (A.5), we obtain

$$I_{n,in} = \frac{C_{in} S + 1/R_S}{g_m + g_{mb}} (I_{n,M_1} + I_{n,R_D}) + I_{n,R_D} + I_{n,RS} \quad (A.6)$$

Assuming all noise sources are uncorrelated, the equivalent input noise current spectral density of the CG-TIA is given by

$$\overline{i_{n,in}^2} \cong \frac{(\omega^2 C_{in}^2 + 1/R_S^2)}{(g_m + g_{mb})^2} (\overline{i_{n,M_1}^2} + \overline{i_{n,R_D}^2}) + \overline{i_{n,R_D}^2} + \overline{i_{n,R_S}^2} \quad (A.7)$$

Substituting the equivalent thermal noise for each noise source, we get

$$\overline{i_{n,in}^2} \cong \frac{4kT}{R_S} + \frac{4kT}{R_D} + \frac{4kT(\gamma g_m + 1/R_D)}{(g_m + g_{mb})^2} (\omega^2 C_{in}^2 + 1/R_S^2) \quad (A.8)$$

Appendix B. Transimpedance gain of the DTIA

Fig. B1 shows the main core of the DTIA, which is the circuit of Fig. 8 without its biasing circuitry. Due to capacitor cross-coupling, $v_{s1} \approx v_{g2}$ and $v_{s2} \approx v_{g1}$, where v_{s1} and v_{g1} are source and gate voltages of M_1 and v_{s2} and v_{g2} are source and gate voltages

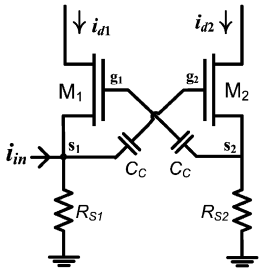

Fig. B1. Capacitor cross-coupling in DTIA.

of M_2, respectively. From the small-signal analysis of the circuit

$$v_{s1} = i_{in}\left[R_{S1}\left\|\frac{1}{(g_{m1}+g_{mb1})}\right.\right] = \frac{R_{S1}}{1+(g_{m1}+g_{mb1})R_{S1}}i_{in} \tag{B.1}$$

since $v_{g2} \approx v_{s1}$, we have Eq. (7) as follows:

$$i_{d2} = \frac{g_{m2}}{1+(g_{m2}+g_{mb2})R_{S2}}v_{g2} = \frac{R_{S1}}{1+(g_{m1}+g_{mb1})R_{S1}} \times \frac{g_{m2}}{1+(g_{m2}+g_{mb2})R_{S2}}i_{in} \tag{B.2}$$

also

$$v_{g1} \approx v_{s2} = \frac{g_{m2}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}}v_{g2} = \frac{g_{m2}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}}\frac{R_{S1}}{1+(g_{m1}+g_{mb1})R_{S1}}i_{in} \tag{B.3}$$

The drain current of M_1, i_{d1}, can be found as follows:

$$i_{d1} = -(g_{m1}+g_{mb1})v_{s1} + g_{m1}v_{g1} \tag{B.4}$$

substituting v_{s1} and v_{g1} from (B.1) and (B.3) into (B.4) yields

$$i_{d1} = \frac{-R_{S1}}{1+(g_{m1}+g_{mb1})R_{S1}} \times \left[\frac{g_{m1}+g_{m1}g_{mb2}R_{S2}+g_{mb1}+g_{mb1}g_{m2}R_{S2}+g_{mb1}g_{mb2}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}}\right]i_{in} \tag{B.5}$$

Assuming $g_{m1} = g_{m2} = g_m$ and $g_{mb1} = g_{mb2} = g_{mb}$, we obtain

$$\frac{i_{d1}}{i_{in}} = \frac{-R_{S1}}{1+(g_m+g_{mb})R_{S1}}\frac{g_m+g_{mb}+2g_mg_{mb}R_{S2}+g_{mb}^2R_{S2}}{1+(g_m+g_{mb})R_{S2}} \tag{B.6}$$

The transimpedance gain of DTIA can be obtained as

$$Z_{T_0}|_{DTIA} = \frac{(i_{d2}-i_{d1})}{i_{in}}R_D \tag{B.7}$$

substituting i_{d1} and i_{d2} from (B.5) and (B.2) into (B.7) yields

$$Z_{T_0}|_{DTIA} = \frac{g_{m2}(1+g_{mb1}R_{S2})+(g_{m1}+g_{mb1})(1+g_{mb2}R_{S2})}{(1+(g_{m1}+g_{mb1})R_{S1})(1+(g_{m2}+g_{mb2})R_{S2})}R_{S1}R_D \tag{B.8}$$

The dc transimpedance gain of CG-TIA is given by

$$Z_{T_0}|_{CG-TIA} = \frac{(g_{m1}+g_{mb1})R_{S1}R_D}{1+(g_{m1}+g_{mb1})R_{S1}} \tag{B.9}$$

Dividing (B.8) by (B.9) yields

$$\frac{Z_{T_0}|_{DTIA}}{Z_{T_0}|_{CG-TIA}} = \frac{1+g_{mb2}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}} + \frac{g_{m2}}{g_{m1}+g_{mb1}} \times \frac{1+g_{mb1}R_{S2}}{1+(g_{m2}+g_{mb2})R_{S2}} \tag{B.10}$$

Appendix C. Noise analysis of the DTIA

Fig. C1 depicts the core of the DTIA, i.e. the circuit in Fig. 9, at high frequencies. $M1$ has a CG configuration while $M2$ is a common-source stage. The contribution in differential transimpedance gain is as follows:

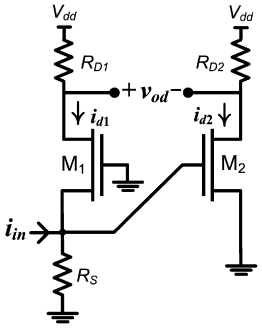

Fig. C1. Core of the DTIA at high frequencies.

$$T_{Z,M_1} = \frac{v_{0d+}}{i_{in}} = \frac{(g_{m1}+g_{mb1})}{(g_{m1}+g_{mb1}+C_{in}S+1/R_S)(C_{out1}S+1/R_{D1})} \tag{C.1}$$

$$T_{Z,M2} = \frac{v_{0d-}}{i_{in}} = \frac{-g_{m2}}{(g_{m1}+g_{mb1}+C_{in}S+1/R_S)(C_{out2}S+1/R_{D2})} \tag{C.2}$$

where C_{in} is the parasitic input capacitance and C_{out1} and C_{out2} are parasitic output capacitances at the drain of M_1 and M_2, respectively. Using (C.1) and (C.2) and assuming $g_{m1} = g_{m2} = g_m$, $g_{mb1} = g_{mb2} = g_{mb}$ and $R_{D1} = R_{D2} = R_D$, differential transimpedance gain is obtained by

$$\frac{v_{0d}}{i_{in}} = \frac{(2g_m+g_{mb})}{(g_m+g_{mb}+C_{in}S+1/R_S)(C_{out}S+1/R_D)} \tag{C.3}$$

From Appendix A, contribution of the left pair of the circuit (Fig. C1) at output noise is

$$V_{n,od+} = \frac{I_{n,R_D}}{C_{out}S+1/R_D} + \frac{(C_{in}S+1/R_S)I_{n,M_1}}{(g_m+g_{mb}+C_{in}S+1/R_S)(C_{out}S+1/R_D)} \tag{C.4}$$

Contribution of the right pair of the circuit at the output noise is

$$V_{n,od-} = \frac{1}{C_{out}S+1/R_D}\left(I_{n,R_D}+I_{n,M_2}+g_m\frac{V_{n,od+}}{T_{Z,M_1}}Z_{in}\right) \tag{C.5}$$

where Z_{in} is the input impedance given by

$$Z_{in} = \frac{1}{g_m+g_{mb}+C_{in}S+1/R_S} \tag{C.6}$$

From (C.3)–(C.5), we have

$$V_{n,od} = V_{n,od+}+V_{n,od-} = \frac{(2I_{n,R_D}+I_{n,M_2})}{C_{out}S+1/R_D} + \frac{R_D(C_{in}S+1/R_S)I_{n,M1}}{(g_m+g_{mb}+C_{in}S+1/R_S)(C_{out}S+1/R_D)} + \frac{g_m}{(C_{out}S+1/R_D)(g_m+g_{mb})} \times \left(I_{n,R_D}+\frac{(C_{in}S+1/R_S)I_{n,M1}}{(g_m+g_{mb}+C_{in}S+1/R_S)}\right) \tag{C.7}$$

Dividing (C.7) by (C.3) yields

$$I_{n,in} = \frac{g_m+g_{mb}+C_{in}S+1/R_S}{2g_m+g_{mb}}\left(\left(\frac{g_m}{g_m+g_{mb}}+2\right)I_{n,R_D}+I_{n,M_2}\right) + \left(\frac{g_m}{g_m+g_{mb}}+1\right)\frac{(C_{in}S+1/R_S)}{2g_m+g_{mb}}I_{n,M_1} \tag{C.8}$$

Including the noise contribution from R_S, (C.8), becomes

$$I_{n,in} = \frac{g_m + g_{mb} + C_{in}S + 1/R_S}{2g_m + g_{mb}} \left(\left(\frac{g_m}{g_m + g_{mb}} + 2 \right) I_{n,R_D} + I_{n,M_2} \right) + \left(\frac{g_m}{g_m + g_{mb}} + 1 \right) \frac{(C_{in}S + 1/R_S)}{2g_m + g_{mb}} I_{n,M_1} + I_{n,R_S} \quad \text{(C.9)}$$

Assuming all noise sources are uncorrelated, the equivalent input noise current spectral density of the DTIA becomes

$$\overline{i_{n,in}^2} \cong \left\{ \overline{i_{n,R_S}^2} + \overline{i_{n,M_1}^2} \frac{(\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m + g_{mb})^2} \left[\left(\frac{g_m}{g_m + g_{mb}} \right)^2 + 1 \right] + \frac{(g_m + g_{mb})^2 + (\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m + g_{mb})^2} \times \left\{ \left[\left(\frac{g_m}{g_m + g_{mb}} \right)^2 + 2 \right] \overline{i_{n,R_D}^2} + \overline{i_{n,M_2}^2} \right\} \right\} \quad \text{(C.10)}$$

Substituting the equivalent thermal noise for each noise source, we get

$$\overline{i_{n,in}^2} \cong 4kT \left\{ R_S^{-1} + \gamma g_m \frac{(\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m + g_{mb})^2} \left[\left(\frac{g_m}{g_m + g_{mb}} \right)^2 + 1 \right] + \frac{(g_m + g_{mb})^2 + (\omega^2 C_{in}^2 + R_S^{-2})}{(2g_m + g_{mb})^2} \left\{ \left[\left(\frac{g_m}{g_m + g_{mb}} \right)^2 + 2 \right] R_D^{-1} + \gamma g_m \right\} \right\} \quad \text{(C.11)}$$

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