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UPFC DC LINK OSCILLATION REDUCTION USING FULL BRIDGE CONVERTER ON DC LINK

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ABSTRACT

This paper proposes a unified power flow controller (UPFC) with a DC-link module composed of a DC-link capacitor and a full bridge converter as a series voltage compensator. The voltage compensator is connected in series with the DC bus line and generates a voltage to eliminate the voltage ripples on the DC-link capacitor. By applying this voltage source converter, the overall required capacitance is reduced allowing the replacement of electrolytic capacitors by alternatives with longer lifetime and reduced volume and cost. The simulation study of the proposed topology is carried out and investigated the effects of DC-link capacitance reduction on output parameters of UPFC by using a series voltage compensator. The complete simulation of model voltage compensator is implemented in MATLAB/Simulink and the results realize that proposed series voltage compensator reduced the DC-link voltage ripples and improved the active and reactive power injection and also reduced the harmonic effects on system.

Keywords— *Unified power flow controller (UPFC); voltage regulation; DC-link capacitor; Full bridge converter; series voltage compensator*

INTRODUCTION

These Flexible AC Transmission Systems (FACTS) devices are based on power electronic controllable devices such as Static Var Compensation (SVC), static synchronous compensator (STATCOM), Voltage Regulating Transformers (VRTs), Static Synchronous Series Compensator (SSSC), Interline Power Flow Controller (IPFC) and Unified Power Flow Controller (UPFC) that have been extended to improve the performance of Alternating Current (AC) transmission in various system application. These devices have been proposed to improve the conventional procedures whit high potential to lower cost, increased flexibility and power transfer capability. Actually FACTS controllers, by providing additional degrees of freedom to control power flows and voltages, narrow the gap between the noncontrolled and the controlled power system operation mode, at key locations of the network [1].

UPFC proposed by Gyugyi [2] is an advanced solid-state converter and one of the most important devices in FACTS concept for the regulation of voltage and power flow optimization in transmission lines [3]. As shown in fig. 1, UPFC consists of two switching power converters which connected as back-to-back with a common DC-link. The DC-link capacitor acts as an energy buffer to stabilize the DC-link voltage and keep it almost constant. When a UPFC is installed in a long-distance transmission line, it may be impractical for the DC-link capacitor to release or absorb all the transient-state active power through the series device [4]. In this case, the shunt device should share the transient-state active power with the DC-link capacitor, or the series device should impose a limitation on the response time of power flow control. DC capacitor is proportional to the line inductance, so that a large capacitor is required for long-distance transmission systems that it can cause the highest cost and volume of the components. Also the DC-link capacitors have an effectively role on the cost, and physical size of the VCSs which occupy 23% of the volume, weight and costs of the converters. Thus manufactures try to reduced its negative effect [5]. So based on [6]–[10], in recent years, there are many papers proposed several methods to reduction of DC-link capacitors for decrease the size and cost of the equipment and increase the controllability of them. By considering the DC-link voltage ripples in UPFC, this paper applied a series voltage compensator to reduction of voltage ripples to reduce the voltage ripple of the DC-link in a UPFC.

This paper is organized as follows. Section II introduces system description, the term “DC-link capacitors” and its application in power converter. The performance of series voltage compensator for cancelation DC-link voltage ripple of UPFC and simulation result are in section III and IV respectively. In section V Concluding remarks are summarized

SYSTEM DESCRIPTION

Among FACTS controllers, the UPFC is a versatile device that can control various system variables independently

A. UPFC Operation

In UPFC, voltage source converters operate as STATCOM and solid-state series controllers (SSSCs) to control the active and reactive power in the line and voltage magnitude of the UPFC’s terminals. The series-connected VSC injects a voltage with both controllable magnitude and phase angle in series with the transmission line, thus provides active and reactive power compensation to the transmission line. The shunt-connected VSC provides the active power drawn by the series branch and

the losses through the common DC-link and also provides reactive compensation to the system independently[7]. The combined version of active and reactive power provides the total complex power of the line. Active power can be calculated by line current in phase with injected voltage and reactive power is calculated by line current quadrature phase with injected voltage.

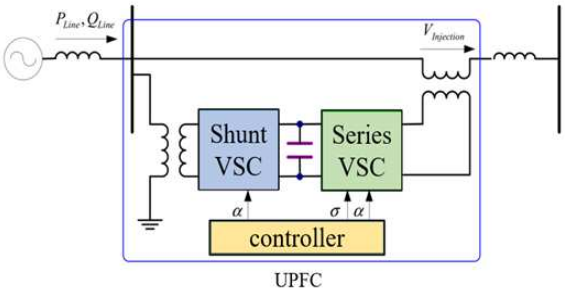

Fig1 UPFC schematic

The combined version of active and reactive power provides the total complex power of the line. Active power can be calculated by line current in phase with injected voltage and reactive power is calculated by line current quadrature phase with injected voltage[1].

$$V_{sa} = V_m \cos\theta_{av} = V_m \cos(\omega t) \quad (1)$$

$$V_{sb} = V_m \cos\theta_{bv} = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \quad (2)$$

$$V_{sc} = V_m \cos\theta_{cv} = V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \quad (3)$$

Hence the expected line side currents in the STATCOM side and the fundamental component of the voltage injected into the transmission line in the SSSC side are described as:

$$I_a = I_m \cos\theta_a = I_m \cos(\omega t - \Psi_{in}) \quad (4)$$

$$I_b = I_m \cos\theta_b = I_m \cos\left(\omega t - \frac{2\pi}{3} - \Psi_{in}\right) \quad (5)$$

$$I_c = I_m \cos\theta_c = I_m \cos\left(\omega t + \frac{2\pi}{3} - \Psi_{in}\right) \quad (6)$$

Where $\Psi_{in} = \theta_{av} - \theta_a$ is the line side power factor angle

$$V_{su} = V_o \cos\theta_{ou} = V_o \cos(\omega t + \varphi_o + \Psi_{out}) \quad (7)$$

$$V_{sv} = V_o \cos\theta_{ov} = V_o \cos\left(\theta_{ou} - \frac{2\pi}{3}\right) \quad (8)$$

$$V_{sw} = V_o \cos\theta_{ow} = V_o \cos\left(\theta_{ou} + \frac{2\pi}{3}\right) \quad (9)$$

Following sections describe the modulation techniques employed for the shunt and series converters and the controllers used for both the shunt and series compensations.

B. DC-link voltage fluctuations

According to [11] Fujita said "when the DC-link capacitor provides the transmitted energy to the series device in transient states, a small kVA rating is required for the shunt device, which is slightly larger than the steady-state power." The DC-link voltage, fluctuates in transient states, according to releasing or absorbing the energy. Then the DC-link capacitor has to be designed to regulate the fluctuation of the DC-link voltage. When the dc voltage changes from V_{dc1} to V_{dc2}, the energy released from the DC-link capacitor, ΔW_{dc} is given by:

$$\Delta W_{dc} = \frac{1}{2} C_{dc}(V_{dc1}^2 - V_{dc2}^2) \quad (10)$$

Where C_{dc} is the capacitance of the Dc-link capacitor. Actually we know that the transmitted energy ΔW is equal to the difference of the stored energy in the line inductor between stage 1 and 2:

$$\Delta W_{dc} = \frac{3}{2} L(I_2^2 - I_1^2) \quad (11)$$

Where L is the line inductance. By defining the ratio of the dc voltage fluctuation, ε is defined as:

$$\varepsilon = \frac{V_{dc1} - V_{dc2}}{V_{dc1}} \quad (12)$$

Substituting (3) to (1) and assumption $\varepsilon^2 \ll 2\varepsilon$ yields the following relation of the required capacitance of the dc-link capacitor:

$$C_{dc} = \frac{3L(I_2^2 - I_1^2)}{2\varepsilon V_{dc1}^2} \quad (13)$$

According to DC-link capacitance equation, the DC capacitor is proportional to the line inductance, so that a large capacitor is required for long-distance transmission systems that it can cause the highest cost and volume of the UPFC.

C. Characteristics of DC-link capacitor

DC-link capacitors are widely used in power converters to balance the instantaneous power difference between the input source and output load, and minimize voltage variation in the DC link. In some applications, they are also used to provide sufficient energy during the hold-up time. As shown in fig. 2 the intermediate stage of the structure is DC-link capacitors which are used to absorb the instantaneous power, between two terminals of the converters, filter the harmonics, and reduce the DC voltage ripple. According to [12] Three types of capacitors are generally available for DC-link option in power electronic applications, as flow: Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps).
The selection of a DC–link capacitor is based on some factors such as: amplitude of the current ripple, voltage variation, electrical and thermal analysis, ect. Based on the technical characteristic of the capacitors such as failure modes, failure mechanisms, corresponding critical

stressors and lifetime, they can be used in DC-link applications. the electrolytic capacitors are the most popular because of their high volumetric efficiency and low cost per unit capacitance, still they suffer from low ripple current capability, short life time, temperature limitations and size [12], [13]. The larger DC-link capacitance is caused the less reliability in equipment. In many applications the electrolytic capacitors have been used as DC-link capacitance. The electrolytic capacitor is a critical component in determining the lifetime of the converter system especially for high-power or high-voltage applications. The problem is that it is large, heavy, expensive and unreliable [14]. Electrolytic capacitors with large capacitance per unit volume have been commonly used as the DC-link capacitors. However, they are bulky and make the converter less reliable because of their short life time expectancy. Moreover, the large DC-link capacitance causes the larger total harmonic distortion (THD) of the input source current. Based on various roles of DC-link capacitor in UPFC, which is mentioned in the previous sections, based on [6], [12] the design of DC links, encounters the following challenge: A) Failure rate of the capacitors are more than other components in equipment. B) The importance of reducing costs for Manufacturers in the entire equipment compared to conventional type without undue risk. C) Consideration some environmental condition such as high ambient temperature or humidity that capacitors are to be exposed them. D) Limit the volume and temperature of the capacitors with the trends for high power density power electronic systems. By considering this challenges, manufactures can evaluation the optimum capacitor to operation of DC-link requirements. Also they must be attending to some other characteristics of capacitors for use in the equipment such as UPFC.

SERIES VOLTAGE COMPENSATOR FOR REDUCTION OF DC-LINK CAPACITOR IN UPFC

This paper uses a concept by introducing a voltage compensator in series with DC-link capacitor. the voltage compensator is used for cancellation of the voltage ripples on DC-link capacitors and partial balance of power.

A. *Series voltage compensator*

Reduction of DC-link capacitance can cause instability the DC-link voltage in UPFC. If the source inductance is large compared to the DC-link capacitance it can be caused over voltage or under voltage faults. By increasing the DC-link voltage the load current is getting smaller so as to maintain constant power to the load. These instability problem can be solved by designing a filter or voltage compensator or other components. one of these components is series voltage compensator, that can be reduced the DC-link voltage ripples. It is connected in series with DC bus lines to eliminate the voltage ripples on DC-link capacitors and partial balance of power in UPFC.As shown in fig. 2 the used series voltage compensator in the UPFC is a full bridge converter which is implemented by four IGBTs, $S_1 - S_4$ and output filter C_f, L_f. The sources for the voltage compensator can be an auxiliary capacitor, external source with a capacitor, or coupled winding with a capacitor.

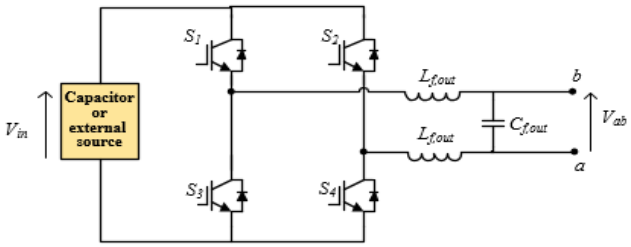

Fig. 2. Circuit structure for the voltage compensator

B. *Control strategy*

The dc-link capacitor V_c is sensed to obtain its ac component and extract its ac component by using a high pass filter (HPF). The input voltage of the compensator (V_{in}) is compared by V_{in}^* where V_{in}^* is the voltage reference for the input voltage of the compensator. A low pass filter (LPF) eliminate the DC offset which may appear in the input voltage of the compensator that can caused non-ideal switching action of the full bridge switches. After LPF the difference between V_{in} and V_{in}^* is processed by a PI controller to give an offset voltage. The control signal (V_{cont}) is derived by combining the output signal of the PI controller and the output of the HPF. The resultant control signal is then as the input of the PWM controller, as shown in fig. 3

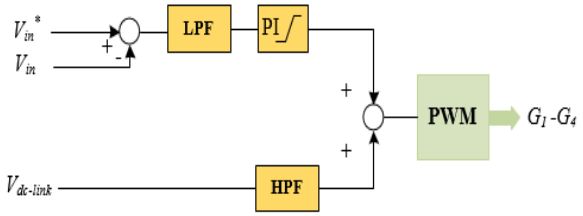

Fig. 3 Control mechanism with a capacitor as the input source of the voltage compensator.

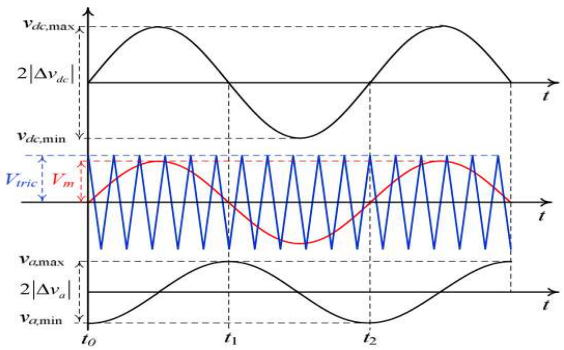

fig. 4. PWM and the ripple voltage generated of the voltage compensator illustrated in [7]

Then as shown in fig. 4, PWM controller is used to compare with the triangular carrier waveform V_{tric} in the PWM modulator to generate the Compensating.

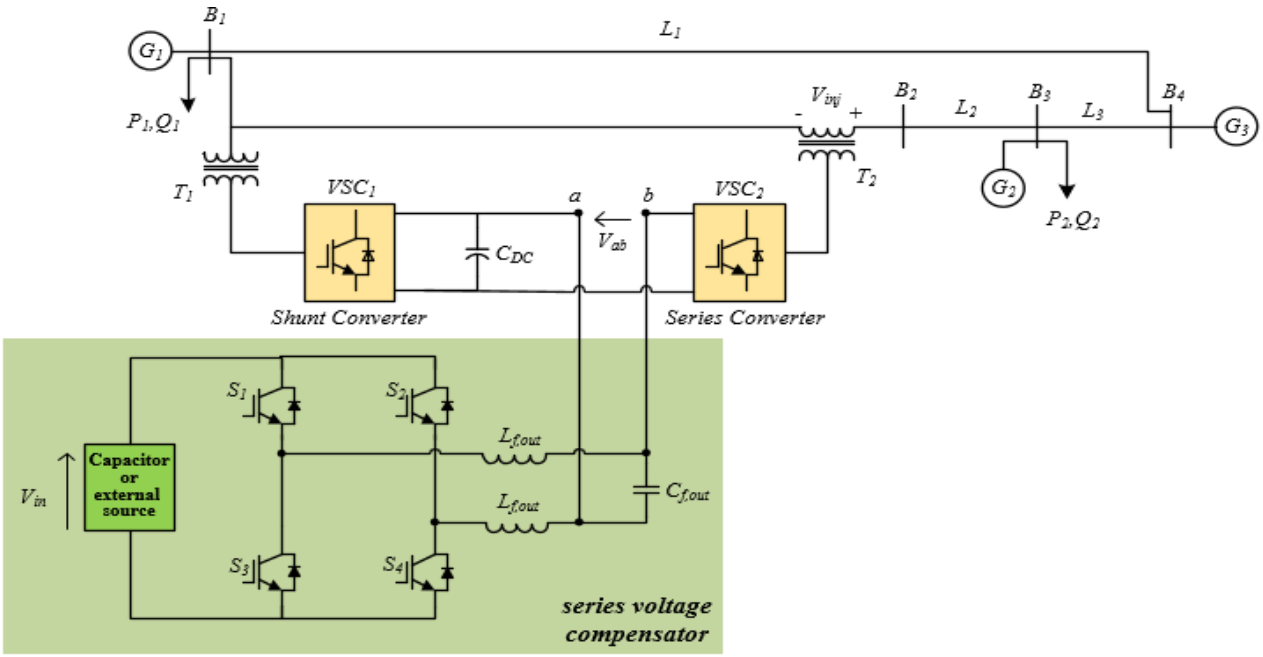

Fig 5 Schematic model of the MATLAB/Simulink system

SIMULATION RESULT

In order to verify the performance of the series voltage compensator, the studied UPFC and the series voltage compensator are simulated in the MATLAB/Simulink environment. The Typical model of the system is illustrating in fig.8. and The parameters used in the simulation are shown in table I.

TABLE I: System Parameters

System parameter	value
V_{grid}	500KV
$S_{load\ ,1}$	300MW
$S_{load\ ,2}$	200MW
$G_1\ , G_2\ , G_3$	8500,6500,9000(MVA)
V_{in}	250 V
$L_{f,out}$	$120\mu H$
$C_{f,out}$	$3.3\mu F$
$C_{DC-link}$	5000 μF
frequency	60Hz

As shown in fig. 5 the UPFC is used in a 500 kV transmission system and located at the left end of the line L_2, between the 500 kV buses B_1 and B_2, is used to control the active and reactive powers flowing through bus B_2while controls voltage at bus B1. It consists of two 870-MVA, three-level GTO-based converters, one connected in shunt at bus B_1 and one connected in series between buses B_1 and B_2. The shunt and series converters can exchange power through a DC bus. The series converter can inject a maximum of 10% of nominal line-to-ground voltage (28.87 kV) in series with line L_2. Also because of DC-link voltage ripples amplitude, V_{in} is considered 250V.

By applying a voltage compensator in series with DC bus lines, the DC-link voltage is compensated and then the voltage ripples and fluctuations of the DC-link have been reduced as shown in fig. 6. By reducing the DC link voltage ripples, the performance of the UPFC is improved. Actually the result of the voltage improvement is appeared as the injection voltage to the bus 2. As shown in fig. 7 before compensating the injection voltage from the UPFC to bus 2 is instable and its THD is 74% which illustrate in fig. 8. after compensation the injection voltage to the B_2 has improved and it verify by attention to THD of the injection voltage (V_{inj}) which is 15.54% and illustrate in fig. 8.

By improving the injection voltage of the UPFC to the B_2 beacause of its effect on the active and reactive power of the line2 as shown in fig. 10 and fig. 11 the ripple of the line active and reactive power has reduced. By considering the active power waveform, the difference of the minimum and maximum power is variable about 2-5MW. But After applying the voltage compensator, the variation is redused about 0.5-1 MW.also before compensation the difference of the minimum and maximum power is variable about 1-4Mvar and after compensating the difference is reduced about 1Mvar as shown in fig. 11.

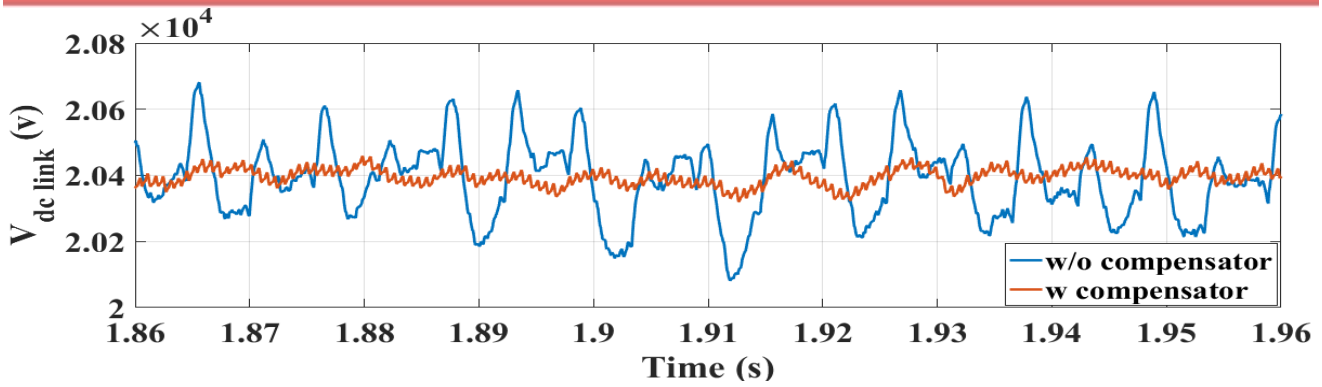

Fig. 6. DC-link voltage ripples, with(red) and without(blue) DC-link voltage compensator

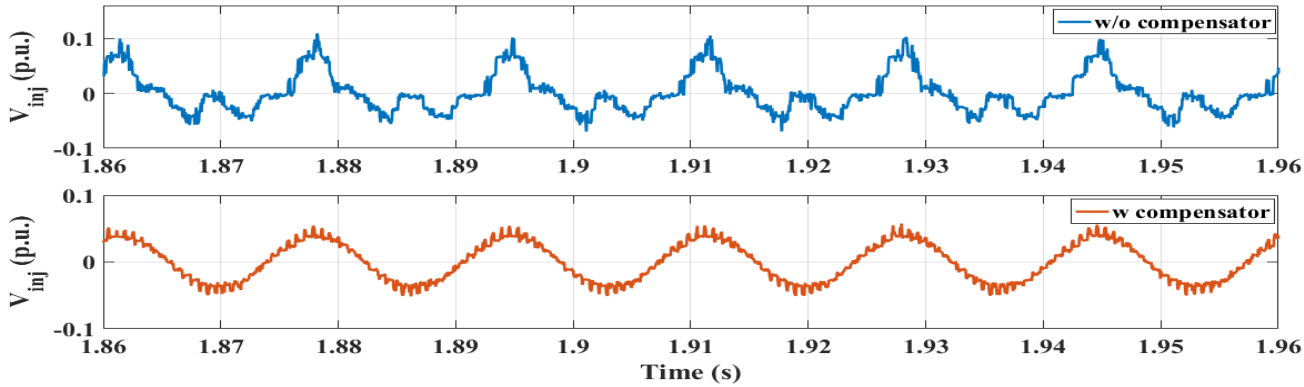

Fig. 7. Injection voltage waveform to bus2 from UPFC, with(red) and without(blue) DC-link voltage compensator

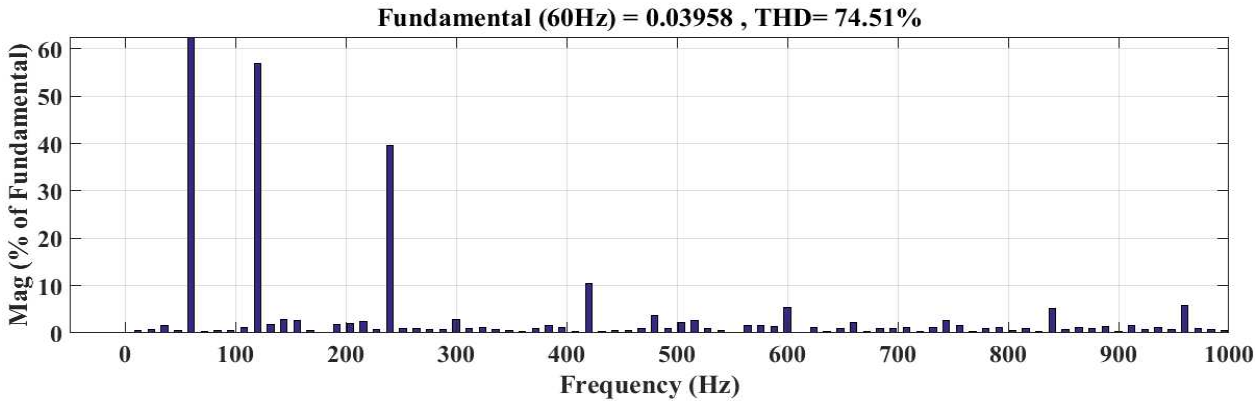

Fig. 8. THD of the V_{inj} before DC-link voltage compensation

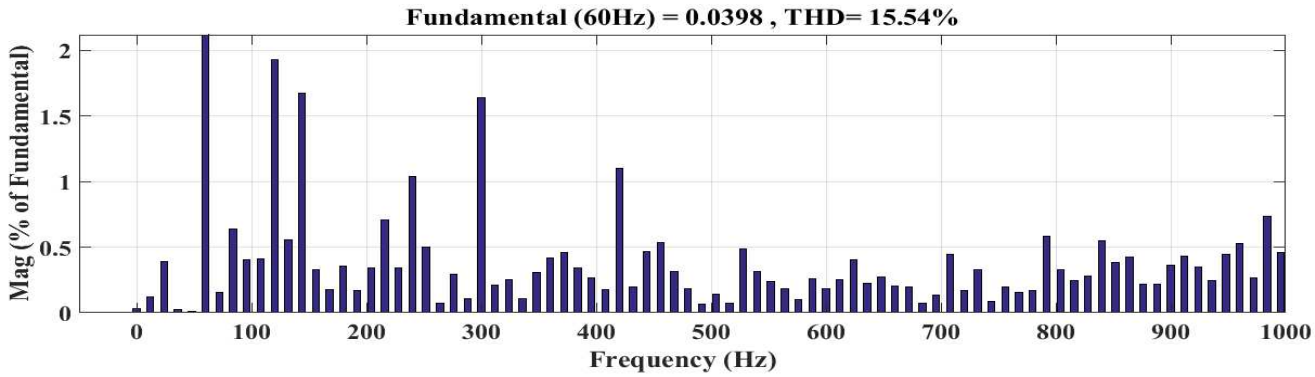

Fig. 9. THD of the V_{inj} after DC-link voltage compensation

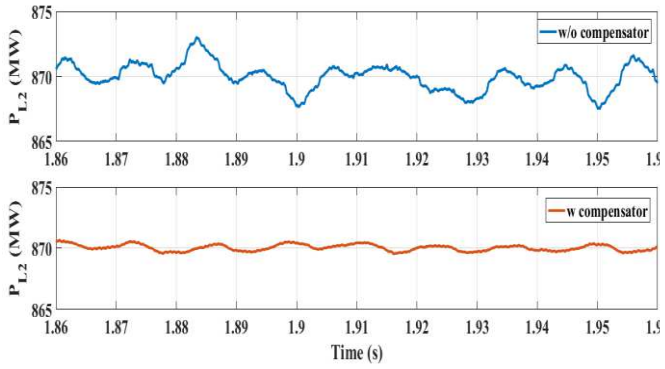

Fig. 9. Output active power of the UPFC, with(red) and without(blue) DC-link voltage compensator

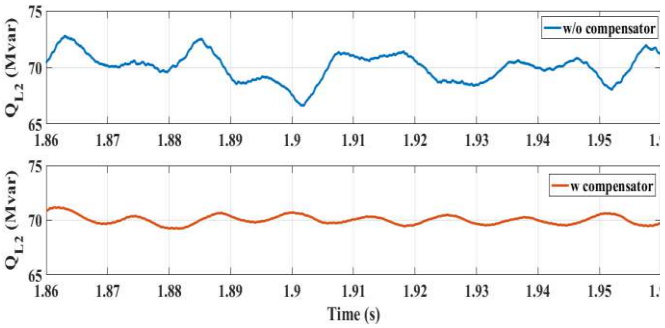

Fig. 10. Output reactive power of the UPFC, with(red) and without(blue) DC-link voltage compensator

Actually the results are shown that series voltage compensator reduced the DC-link voltage ripples and also improved the injection voltage waveform from UPFC to bus2. Thus by improving the injection voltage to bus 2, the UPFC's performance and power flow control of the grid can have improve.

CONCLUSION

The contribution of this paper is to propose a solution for reduction of the bulky DC-link capacitor by using a series voltage compensator. Since the cost occupied by the DC link capacitor in the existing UPFC structure are quite large, the proposed scheme reduces the DC link capacitor size. The proposed series voltage compensator has been applied to compensate the DC-link voltage after reduction of DC-link capacitor in UPFC application. The results are realized that the DC-link voltage and injection voltage of the SSSC and also active and reactive power to transmission line have improved. The series voltage compensator offers improved DC-link voltage ripples and the THD of the injection voltage from UPFC to transmission line. Actually, by reducing capacitance of the DC-link in UPFC and after compensation DC-link voltage, the performance of the UPFC has improved

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