Optimal Switching Algorithm for Different Topologies of 15-Level Inverter Using Genetic Algorithm

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***Abstract*— Multi-level inverters (MLIs) have better power quality factors compared with two level inverters, because of their staircase output waveform. Switching algorithm and Total Harmonic Distortion (THD) of the MLIs are important issues in the MLI operation. In this paper, THD and switching algorithm of three 15-level inverters topologies are investigated. In order to obtain their optimal switching algorithm, a THD-based objective function for output voltage waveform is expressed and optimized by using Genetic Algorithm (GA). Simulation of these topologies in MATLAB/Simulink is carried out to validate the results of GA. As shown in the paper, asymmetrical 15-level inverter has better performance than other topologies.**

***Index Terms*--15-level inverter, genetic algorithm (GA), different topologies, total harmonic distortion (THD).**

I. INTRODUCTION

Multi-Level Inverter (MLI) has been developed due to high voltage operating capability, good power quality and reduced Electro Magnetic Interface (EMI) [1]. The MLI can use renewable energy resources such as Photovoltaic (PV) and green energies such as Fuel Cells (FCs). Due to the staircase voltage output waveform, the MLI produces lower harmonics and better power quality for output voltage rather than two level ones. Moreover, lower switching frequency of MLI switching devices leads to better efficiency and lower switching loss [2-5]. Some of MLI advantages can be seen in Fig.1.

The concept of MLI has been developed in the last decades [5] and different topologies of them have been introduced. There are three main MLI categories: Cascaded H-Bridge inverters (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FLC). Among them, NPC and FLC need more diodes and capacitor, respectively. Therefore, CHB has advantage over NPC and FLC and it is built from two or more modules of H-Bridges (HBs) without using additional devices. Each H-Bridge has two legs including four switches in their structures [7-9].

CHBs are categorized in two major classes according to voltage sources: Symmetrical MLI (SMLI), which including equal DC voltage sources, and Asymmetrical MLI (AMLI), which uses unequal DC voltage sources. In order to have equal output voltage levels, SMLI has more DC voltage sources and also need more number of switches that increases its complexity and investment cost. One of the advantages of SMLI is their modularity where AMLI has not this characteristic.

There are different proposed structures in literatures that need lower number of switches [10-16]. In [10], a new MLI with bidirectional switches has been introduced. By connecting DC voltage sources in series and parallel with it, a new MLI has been introduced in [11]. In [15-16], the proposed MLI has lower number of switching devices compared with conventional MLI.

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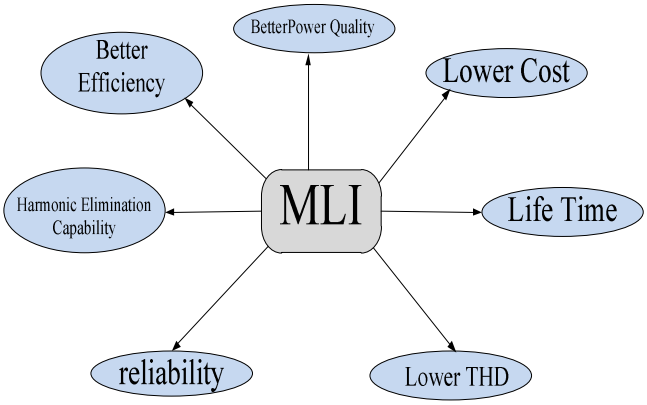


Fig. 1: Schematic of some MLI advantages.

In order to achieve switching algorithm using Different Pulse Width Modulation (PWM), different methods have been studied such as Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM) and Multi Carrier PWM (MCPWM) in [17-19]. There are two methods for investigating switching algorithm based on harmonic distortion

In the some of them, Selected Harmonic Elimination (SHE) has been applied to achieve switching algorithm by introducing a mathematical term and solved by numerical methods such as Newton-Raphson or evolutionary algorithms such as Genetic Algorithm (GA) [20, 23]. On the other hand, some papers have studied other goals such as minimization of Total Harmonic Distortion (THD). In these papers, a THD-based objective function for switching angles has been introduced and solved by numerical or evolutionary algorithms [20-22].

In this paper, three topologies of 15-level inverter including SMLI, AMLI and a new topology, which is introduced in [16], are investigated. At first, their topologies and switching patterns are introduced and then, a THD-based objective function is defined. The GA is used to minimize THD of them. In order to validate the GA results, simulations of three topologies are carried out by MATLAB/Simulink. A comparison between these topologies, based on the results of simulations and their structures, are presented in Section V.

II. 15-Level Inverter

A. *Symmetrical 15-level inverter*

A symmetrical 15-level inverter consists of seven HBs. These HBs have equal DC voltage sources. Topology of symmetrical 15- level inverter and output voltage waveform are shown in Fig. 2. IGBTs or MOSFETS can be used as the switching devices of this structure.

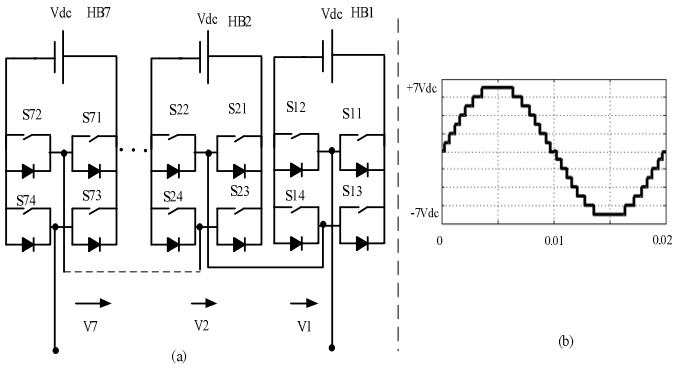


Fig. 2. a) Topology of symmetrical 15- level inverter; b) output voltage waveform

Output voltage of this MLI can be expressed as follows:

$$V_{oN} = \sum_{i=1}^{m} V_{oi} \qquad (1)$$

where V_{oi} is the voltage of each HB and m is the number of HB which is seven in this structure. Each HB can produce three voltage levels ($+V_{dc}$, 0, $-V_{dc}$). By appropriate control of HBs switches, different voltage levels can be achieved from $+7*V_{dc}$ to $-7*V_{dc}$: (+7, +6, …, +1, 0, -1…, -6, -7) * V_{dc} . For this purpose, one of the HBs is activated in each level. For example, to achieve 5 V_{dc}, five HBs should generate $1V_{dc}$ and two HBs should generate zero.

B. *Asymmetrical 15-level inverter*

As shown in Fig. 3, the asymmetrical 15-level inverter consists of three unequal DC voltage sources: $1V_{dc}$, $2V_{dc}$ and $4V_{dc}$. Three HBs are connected in series and output voltage can be calculated using (1) where m=3. Output voltage waveform has seven positive levels, seven negative levels, and a zero one. The output voltage of 15-level inverter in one positive half cycle is shown in Fig.3. The negative half cycle is similar to positive one. As it can be seen, seven switching angles (α_1, α_2, .. , α_7) should be determined to know output waveform of structure. In order to achieve each voltage level in output waveform, these three HBs should be used. Table 1 determines the switches that should be turned on for a half cycle to generate each voltage level. The angles can be each value lower than 90° and it is important to determine optimal angles for minimum THD. It should be noted that the output waveform of asymmetrical inverter is similar to symmetrical one.

Table 1: Switching pattern for the one half of a cycle

Switches that should be turned on for the first 90^0 operation	Output voltage level
S11, S14, S21, S23, S31, S33	$1V_{dc}$
S11, S13, S21, S24, S31, S33	$2V_{dc}$
S11, S14, S21, S24, S31, S33	$3V_{dc}$
S11, S13, S21, S23, S31, S34	$4V_{dc}$
S12, S14, S21, S23, S31, S34	$5V_{dc}$
S11, S13, S21, S24, S31, S34	$6V_{dc}$
S11,S14,S21,S24,S31,S34	$7V_{dc}$

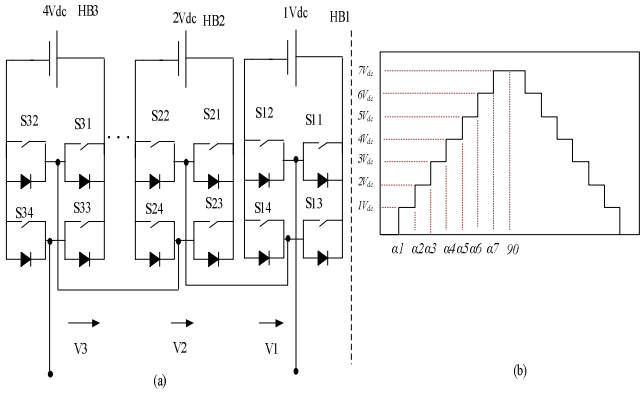


Fig. 3. a) Topology of asymmetrical 15-level inverter; b) A half cycle of output voltage waveform.

C. *A new 15-level inverter proposed in [15]*

The general topology of MLIs has been introduced in [16]. This MLI needs bi-directional switches and therefore, the total switching devices which are used in this topology have been reduced. The 15-level inverter which is proposed in [16], is shown in Fig. 4. In this topology, seven DC voltage sources are used. Table 2, shows the state of switching devices in a half of cycle.

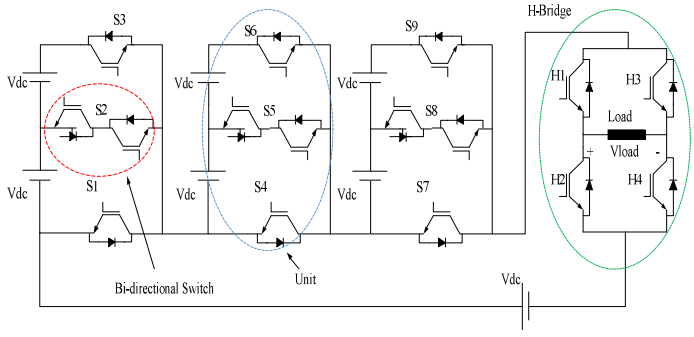
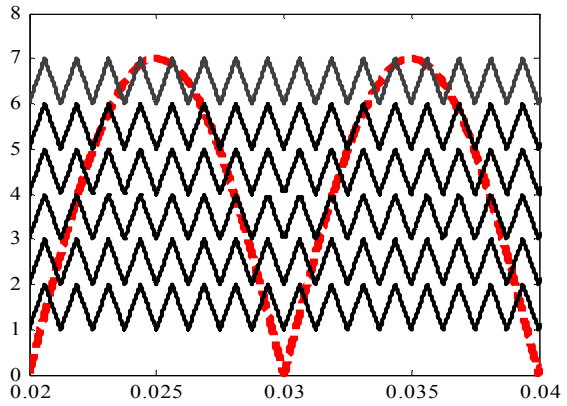


Fig. 4. The new topology of 15-level inverter proposed in [16].

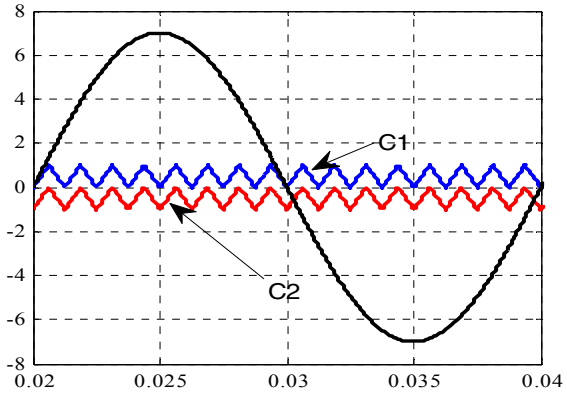
Table 2. Switching pattern of 15-level inverter proposed in [16]

Output voltage	$1V_{dc}$	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$7V_{dc}$
The switching devices which are on	S_1, S_4, S_7, H_1, H_4	S_2, S_4, S_7, H_1, H_4	S_3, S_4, S_7, H_1, H_4	S_3, S_5, S_7, H_1, H_4	S_3, S_6, S_7, H_1, H_4	S_3, S_6, S_8, H_1, H_4	S_3, S_6, S_9, H_1, H_4

In this topology, the multi-carrier pulse width modulation (MCPWM) method has been used. This method is based on comparison of reference wave (sinusoidal) with triangular waves. In order to switching of this structure, six triangular and a sinusoidal wave are used as shown in Fig. 5. In addition, Fig. 5 shows the operation of sine and rectangular waves for switching of a HB. If the value of the sine wave is higher than C1, H1 and H2 are on and if it is lower than C2, H3 and H4 are on. It should be noted that when H1 and H3 are on, zero voltage level is produced.



(a)



(b)

Fig. 5. Modulation waveforms for switching: (a) The waveforms which are used in Fig. 4; (b) The operation of switching devices for a HB.

In this case, frequency of rectangular waves is an important factor for output voltage waveform. mf, which called as frequency index modulation, is defined as follows:

$$m_f = \frac{f_{triangular\ wave}}{f_{sine\ wave}} \quad (2)$$

If m_f is lower than 21, it is usually an odd number. If it is more than 21, it can be odd or even [16].

III. Objective Function

As mentioned before, the switching angles has remarkable influences on the output voltage waveform and its THD. In this paper, in order to obtain and compare the THD and switching angles of three mentioned topologies of 15-level inverter, an objective function based on THD is defined. The output voltage of first two topologies, symmetrical and asymmetrical inverter, are completely similar. Output voltage of such MLI can be expressed as follows:

$$V_o(t) = \left[\sum_{n=1}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_7))\right] \quad (3)$$

where V_{dc} is the amount of the smallest DC source and n is the number of harmonics. In addition, the fundamental component and THD can be obtained as follows:

$$V_{o1} = \frac{4V_{dc}}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_7))\sin(\omega t) \quad (4)$$

$$THD = \sqrt{\frac{V_{orms}^2 - V_{o1rms}^2}{V_{o1rms}^2}} \quad (5)$$

In this paper, GA [20-24] is used for minimization of the objective function. By using (4) and (5), THD of output voltage for symmetrical and asymmetrical inverter can be calculated. For the proposed 15-level inverter in [15], THD of output voltage can be determined by knowing m_f. So, m_f should be optimally determined. Because of m_f, we cannot define an explicit mathematical expression easily. Therefore, in order to calculate the THD of this topology, MATLAB/Simulink has been used and a link between GA and Simulink is applied. In each iteration of optimization, the result of GA (m_f) is used in MATLAB/Simulink to determine the THD of output waveform for this m_f.

IV. Simulation Results

In order to investigate different topologies of the 15-level inverters, optimization and simulations are carried out in this section. At first, by using GA, switching angles and m_f *are* obtained. Then, the results of GA are used in simulations of 15-level inverters in MATLAB/Simulink to validate the GA's results.

4. GA Results

1) The fisrt two topologies

As mentioned before, although symmetrical and asymmetrical 15-level inverter topologies are different from each other, their output voltage is similar. Consequently, both of them have same switching angles in THD minimization study. GA is run for (3) and seven unknown angles (α_1, α_2, .. , α_7) are determined by minimizing the THD-based objective function. Each chromosome (possible answer), have seven genes that represent these angles. The boundary condition of angles are as follows:

$$\alpha_1 \le \alpha_2 \le \alpha_3 \le \alpha_4 \le \alpha_5 \le \alpha_6 \le \alpha_7$$

$$0 \le \alpha_i \le \frac{\pi}{2}, \qquad i = 1, 2, ..., 7$$

In order to optimize THD-based objective function, 40 runs are carried out. Table 3 and Table 4 show the results of these different runs and angles for the best results, respectively. It should be noted that the maximum iteration and tolerance function are set to 100 and 10^{-6}, respectively.

Table 3. Results of GA for AMLI and SMLI

Method	Minimum THD	Maximum THD	Mean THD
GA	%6.5219	%5.27559	%5.5227

Table 4. Angles of best result

angles	α_1	α_2	α_3	α_4	α_5	α_6	α_7
value	4.0930	12.5929	20.1916	28.8119	38.3264	50.2709	64.1602

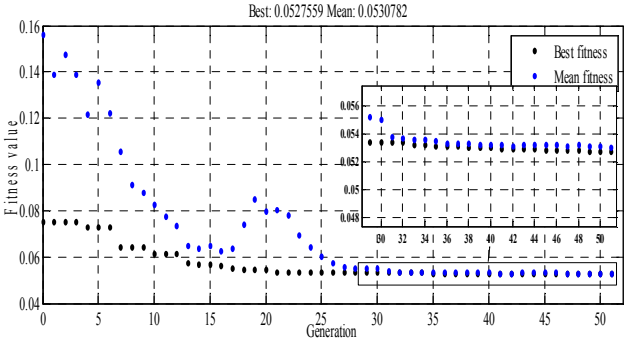


Fig. 6. GA results for minimum THD achieved for symmetrical and asymmetrical 15-level inverters

2) The proposed topology in [15]

For the proposed 15-level inverter in [16], m_f should be determined. In this problem, in order to achieve the THD of output voltage as the objective function, THD block in Simulink is used. Since in each iteration, objective function should be calculated several times, for each gene (m_f *which* is a possible response) Simulink file is run and THD is calculated. GA is run for 40 different runs and the results are

shown in Table 5. The minimum THD achieved by GA for m_f =32 is 6.7862 %. Fig. 7 shows the best and mean values of GA in different iterations of a run.

Table 5. Results of GA for new 15-level inverter

Method	Minimum THD	Maximum THD	Mean THD
GA	% 7.6494	% 6.7862	% 7.217

B. *Simulations of 15-level inverters*

The mentioned topologies of 15-level inverters are simulated by MATLAB/Simulink to validate the results of GA. Fig.8 shows the output voltage waveform using these results. Figs. 9 and 10 show Fourier analysis of output voltage waveform of these topologies. Obviously, it can be seen that voltage harmonic in new MLI is more than other topologies. In addition, the THD, which is obtained from these analyses, is almost similar to the results of GA. The results of simulation show that the output of symmetrical and asymmetrical inverter has the minimum THD in comparison with another topology.

To compare three mentioned topologies, it is seen that symmetrical 15-level inverter has 7 HBs and 28 switches while asymmetrical one has 3 HBs and 12 switches that leads to lower costs. Due to mentioned reasons, asymmetrical 15-level inverter has lower cost and better output voltage THD compared to two other topologies.

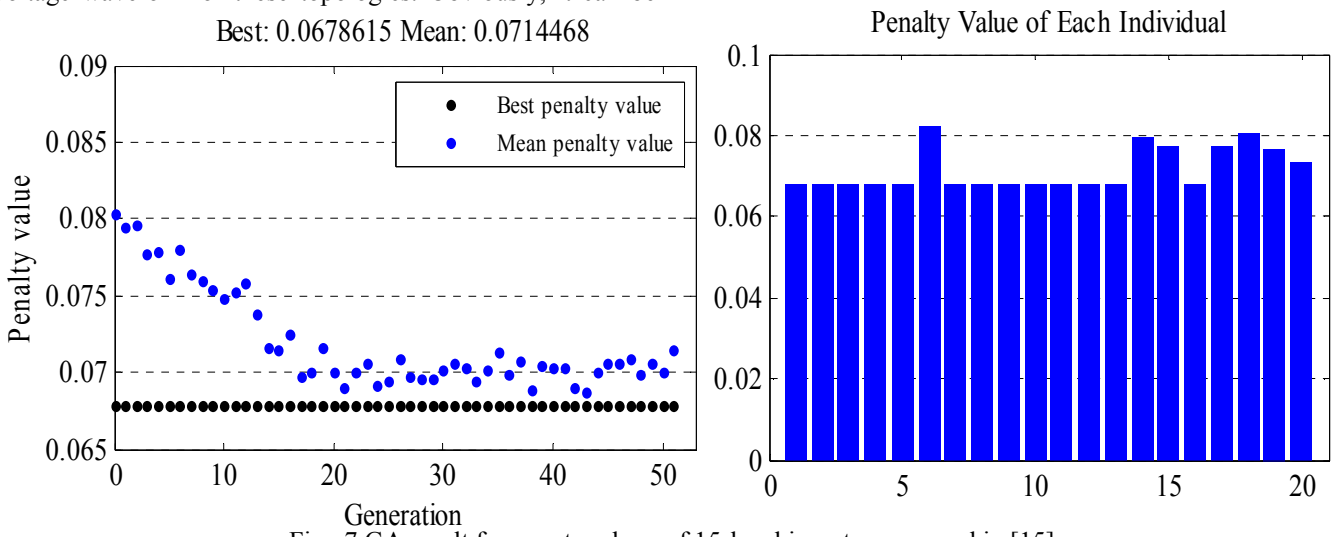


Fig. 7 GA result for new topology of 15-level inverter proposed in [15]

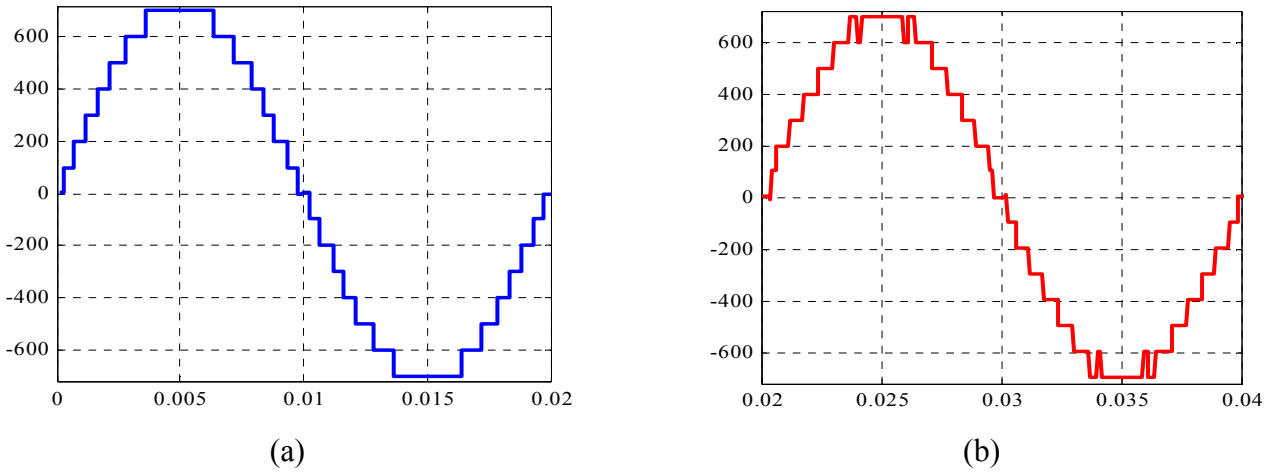


Fig. 8 output voltage waveform for a: symmetrical and asymmetrical 15-level inverter and b: new topology

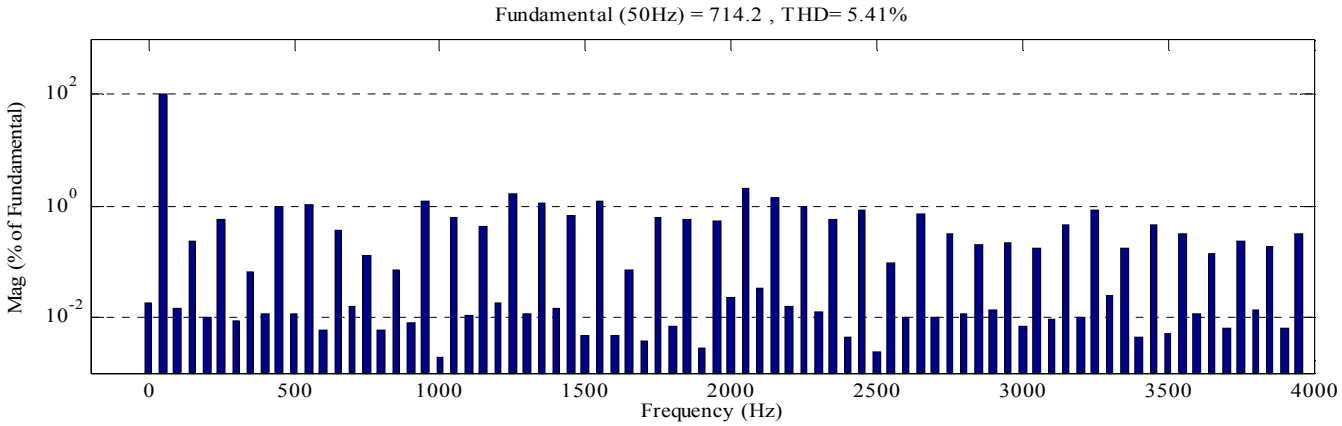


Fig. 9. FFT analysis of voltage of the first two topology

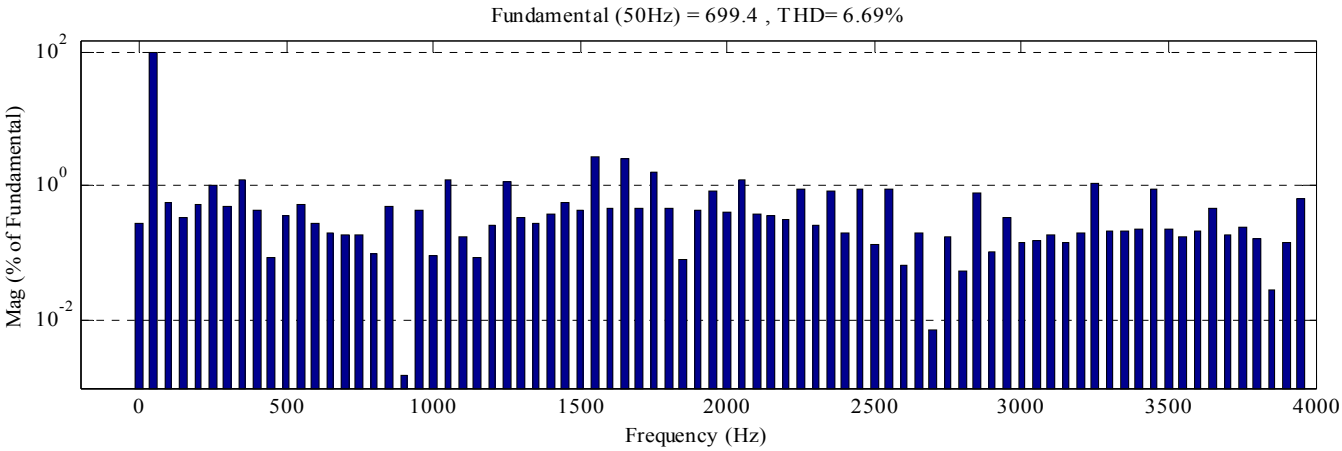


Fig. 10. FFT analysis of voltage of the new topology proposed in [16]

V. COCNLUSION

In this paper, three different topologies of 15-level inverter are investigated. In order to obtain their switching algorithms, a THD-based objective function is defined. Comparisons among results of the simulations show that two first topologies have lower output voltage THD. In addition, comparison between the numbers of required components, which influence the total cost for the topologies, show that asymmetrical 15-level inverter is better than others.

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