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Optimum Design of RF-to-DC Energy Conversion Circuits for Wireless Powered Applications

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Abstract— **In this paper, RF-to-DC voltage rectifier and multiplier circuits for RF power harvesting have been thoroughly investigated. Based on pre-biasing scheme of rectifying devices, a method for their optimum design is presented resulting in improved efficiency in terms of higher output voltage. The impact of positive and negative gate biasing voltage is analyzed and are compared and then possible circuits for their implementation are proposed. It is shown that a negative gate bias is very effective for scavenging ultra-low RF power levels while a positive gate bias can prove useful for high input power levels. All the circuits are implemented in a 180 nm standard CMOS process. The bulk terminal of PMOS and NMOS transistors are connected to the output and reference ground, respectively, to prevent turning the drain and source junction diode of the transistors on.**

Keywords-RF Energy Harvesting; Dynamic Body Bias; Voltage Multiplier

I. INTRODUCTION

Nowadays RF-powered devices have attracted increasing attention in a wide variety of applications such as wearable electronic devices, biomedical implantable devices, passive radio frequency identification (RFID) and internet of things (IOT). RF-powered devices do not require any internal source and collect their required power from the propagating radio frequency waves in the surrounding environment. Almost in all of these applications, an RF-to-DC power conversion circuit is required to extract as much DC power as possible from the incident electromagnetic waves. The ultra-high frequency (UHF) ISM bands are now commonly used for RF energy harvesting. However, it should be noted that the concept of wireless energy transferring and harvesting is not new as it was first demonstrated about 100 years ago by Tesla [1].

An RF energy harvester is composed of three main sub-blocks: an antenna that receives the incident power, an impedance matching network at the interface between the antenna and the circuit, and a voltage rectifier-multiplier, which converts the received high-frequency RF signal at the antenna to a DC voltage and then multiply it to either directly supply the load or to be stored on a storage capacitor. Like other RF circuits and systems, a matching network is required between the antenna and the rectifier to make sure that the maximum power is transferred.

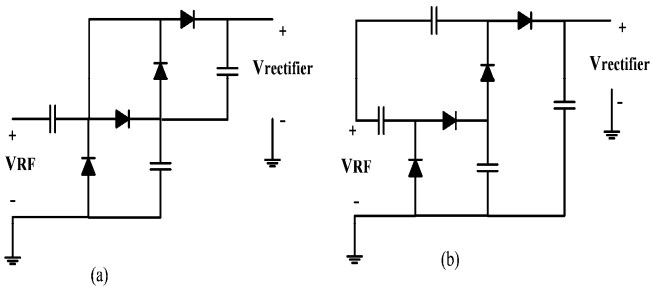

Figure 1. The structure of the (a) Villard and (b) Dickson RF-to-DC voltage rectifiers/multipliers.

To generate sufficient voltages for powering passively powered devices from ultra-low RF power level, the voltage multiplier circuits have been found efficient being a popular subject for RF energy harvesting researches [2]. The two well-known mostly employed topologies for both rectifying and multiplying the RF signals are Villard and Dickson voltage multipliers as shown in Fig. 1(a) and (b), respectively, where the V_{RF} signifies the input AC voltage amplitude and the $V_{rectifier}$ denotes the output DC voltage.

Both Villard and Dickson voltage multipliers do not acquire substantial difference in performance [3]. So, one can choose Villard topology as the millstone for investigations and optimizations as in this work. This paper is organized as follows. Section II discuses about possible configurations of the Villard voltage doubler and then presents a method to improve its functionality in response to RF input signals based on a proposed pre-biasing scheme. Section III deals with the simulation results and finally Section IV concludes the paper.

II. PROPOSED ARCHITUCTURES

The RF signal is an AC signal in nature and thus for obtaining a DC output signal, a rectifier circuit is required. A storage capacitor is also needed to store the extracted power making it available once needed.

A. Conventional Villard voltage doubler

Fig. 1(a) shows the conventional Villard voltage doubler in which diodes are used as rectifying device. The objective of a voltage multiplier is to first rectify its input voltage and then by using multiple sequential stages, prepare the required boosted

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voltage level at its output. The voltage at the output of the n^{th} stage of the Villard voltage multiplier is twice the input voltage amplitude V_i that is received at the input of the first stage, minus twice the threshold voltage of the diodes V_d multiplied by the number of stages n as follows

$$V_n = 2.n(V_i - V_d). \quad (1)$$

However, when supplying a load, the output voltage drops down due to the output capacitor discharge by the load. The output voltage V_{out} of an n-stage Villard voltage multiplier supplying the load R_L can also be defined using the following equation

$$V_{out} = \frac{nV_o.R_L}{nR_o + R_L} = \frac{V_o}{\frac{R_o}{R_L} + \frac{1}{n}}, \quad (2)$$

where, V_o stands for the output voltage of a single stage Villard rectifier under no load condition and R_o is the forward biased resistance of the rectifying diodes [2]. One of the fundamental requirements of energy harvesting circuits is their capability to operate with weak input RF power. As the peak voltage of the AC signal obtained at the antenna is generally much smaller than the threshold voltage of the diode [2], other rectifying devices with lowest possible turn on voltage are preferred.

B. Villard voltage doubler in standard CMOS process

As diodes with low threshold voltage (i.e. Schottky diodes) are not available in standard CMOS processes, the rectifier diodes are replaced with MOS devices. Fig. 2(a) shows a conventional Villard voltage doubler using n-channel MOS (NMOS) transistors and Fig. 2(b) presents a p-channel MOS (PMOS) version of this circuit. The NMOS version may not be suitable for low voltage amplitudes of the input signal as MN2 experiences body effect, which rises its threshold voltage. In contrast, the bulk PMOS devices is under our control due to the fact that PMOS are placed in an n-well inside the p-type substrate. In this circuit the bulk of PMOS devices has been connected to their source terminal. However, for the large amplitudes of the input signal, the drain-bulk junction diode of PMOS transistors turns on providing a path for discharging the C_{out} and thus the output voltage drops. For resolving this issue, one can connect the bulk of PMOS transistors to their drain as shown in Fig. 2(c). However, still in low voltage amplitudes of the input its performance is not well satisfying requiring additional circuit techniques for performance improvement. In the next step, it is possible to replace the MP1 in Fig. 2(c) with a NMOS transistor as the NMOS devices are faster than PMOS counterparts due to higher mobility of electrons (Fig. 2(d)).

Using the pre-biasing of the gate of the rectifying devices by a positive voltage has been already considered as a method to improve the circuit efficiency [4] , [5]. The required positive biasing voltage is derived from the output rectified voltage using a resistive voltage division. However, the resistive branch also acts as a discharging path of the C_{out} at the output. None of previous work have investigated biasing the gate of PMOS transistor with a negative voltage. To thoroughly investigate the impact of pre-biasing the rectifying devices on the circuit performance, as shown in Fig. 3, a biasing voltage V_{bias} is

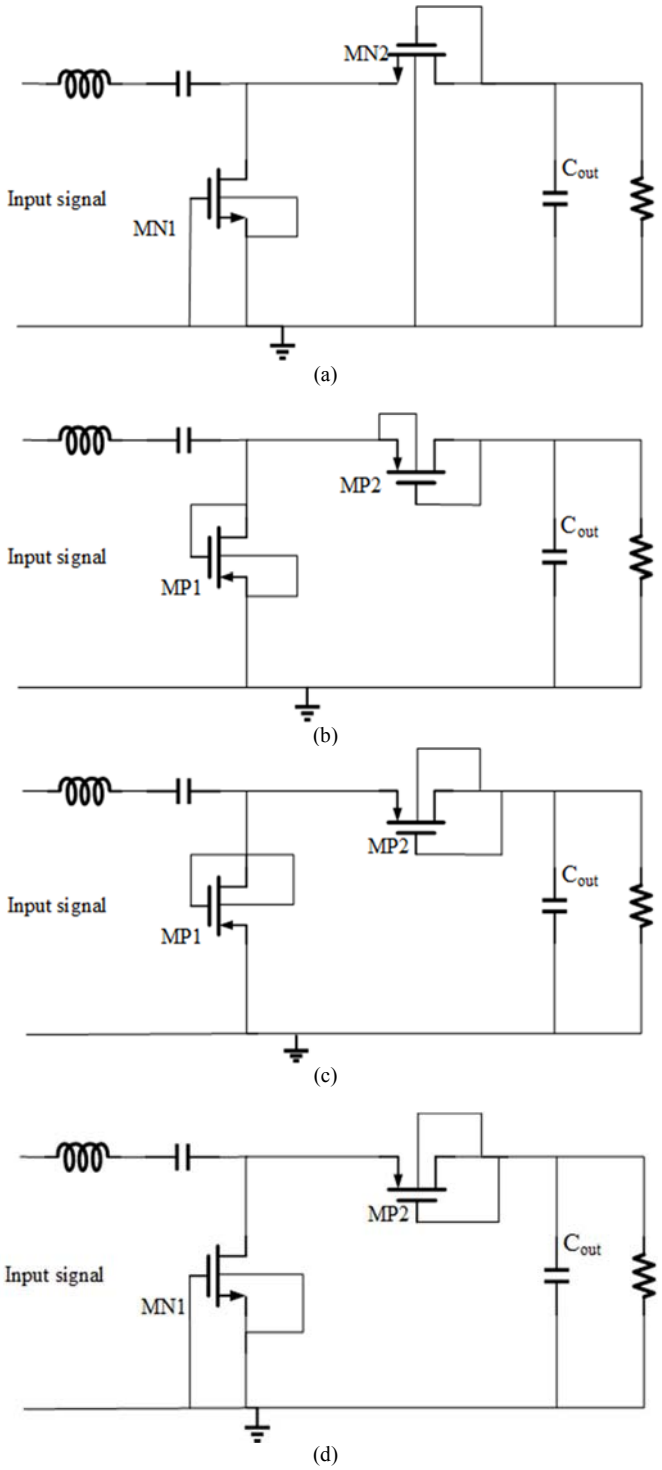

Figure 2. Various configurations of the Villard voltage doubler; (a) using NMOS transistors, (b) a PMOS version with bulk terminals connected to the source terminals, (c) connecting the bulk terminals to the drain to prevent forward biasing of the drain-bulk junction diode, and (d) replacing MN1 with a NMOS one to benefit the higher speed of NMOS transistors due to their higher electron mobility.

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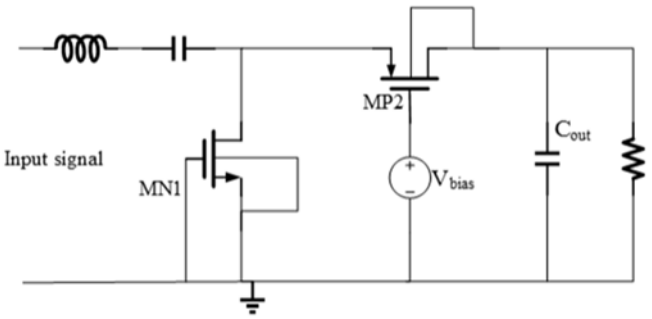

Figure 3. Principle of pre-biasing technique.

applied to the gate of the PMOS transistor. It can be shown that when the input voltage amplitude is below the threshold voltage of the transistors, applying a negative pre-biasing voltage can significantly improve the output voltage of the multiplier. The reason is that when the input voltage is in its positive half cycle, MP2 turns on more easily due to higher gate-source voltage compared with the conventional case where the gate of MP2 is connected to the reference ground. However, if the input voltage amplitude exceeds the threshold voltage of the transistors, applying a positive voltage proves more useful since it helps reduce the leakage current through the MP2 during negative half cycle of the inputs.

As shown in Fig. 4(a), the negative pre-biasing voltage can be realized by a diode connected PMOS in series with a capacitor, acting as a half-wave rectifier. The transistor MP3 is configured so that in negative half cycles of the input signal, it turns on and biases the gate of MP2 with a negative voltage. Note that there is not any load current drawn from C_N, thus a simple half-wave rectifier can do the job efficiently. Alternatively, for generating a positive pre-biasing voltage, it is possible to simply change the direction of MP3 as illustrated in Fig. 4(b).

III. Simuation Results

To verify the proposed pre-biasing technique, the circuits are realized and simulated using TSMC 0.18 μm technology. A 20 pF storage capacitor and a 1 MΩ loading resistor are considered at the output of all circuits. Using the proposed design, at low voltage amplitudes, improvement in output voltage can be observed by a negative pre-biasing voltage and at large voltage amplitudes, a positive V_{bias} is preferred.

Fig. 5 shows the output voltage of the Villard circuit with a pre-biasing gate bias voltage (shown in Fig. 3) with a 1 V, 900 MHz sinusoidal input signal amplitude assuming the V_{bias} varies from −1 V up to +1 V. Apparently, as the V_{bias} increases the output DC voltage also increases so that at V_{bias} = +1 V, V_{out} is nearly twice the input voltage amplitude.

The output voltages assuming a 200 mV input signal amplitude at different negative pre-biasing voltage is shown in Fig. 6. The V_{bias} is assumed to vary from −200 mV to +200 mV in 50 mV steps. It proves that a negative biasing voltage of the MP2 enhances the output voltage.

Fig. 7 and Fig. 8 compare the output voltages of different possible configurations of the Villard voltage doubler shown in Fig. 2 along with the proposed configurations which utilizes pre-

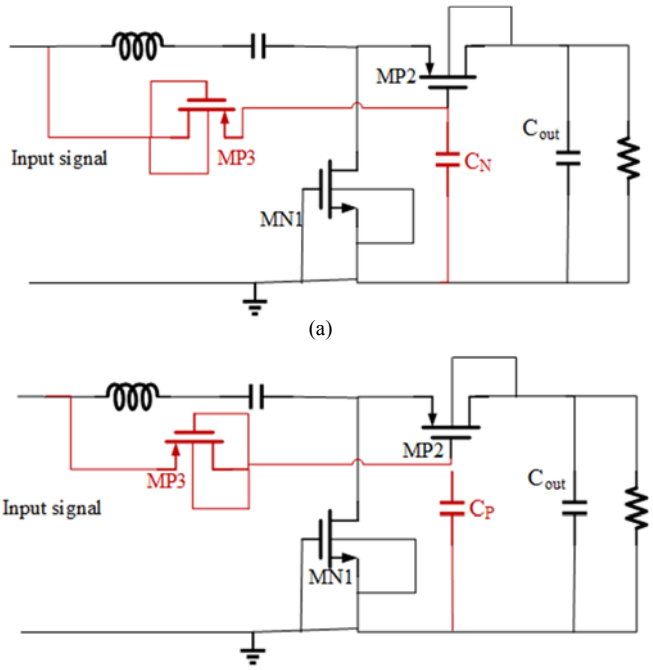

Figure 4. Implementation of the pre-biasing technique in Villard voltage doubler using an extra half-wave rectifier by generating; (a) a negative pre-biasing voltage, and (b) a positive voltage, at the gate of MP2

biasing technique as realized in Fig. 4(a) and (b). The comparison is performed for different amplitudes of the input signal revealing that the proposed structure has better performance compared to conventional configurations. In Fig. 7, it is assumed that the amplitude of the input voltage (i.e. 0 V~ 0.4 V) always remains less than the threshold voltage of the rectifying devices which is about 0.5 V. In contrast, Fig. 8 supposes that the input voltage amplitude is strong enough (i.e. 0.6 V~ 1 V) so that it exceeds the threshold voltage of the rectifying transistors.

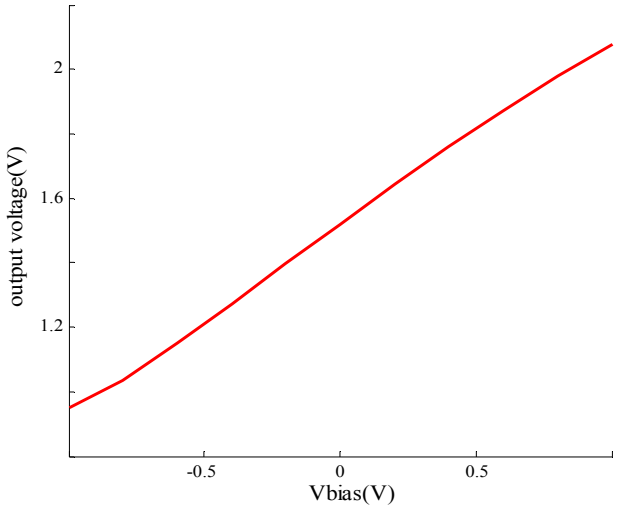

Figure 5. Output DC voltage of Villard voltage doubler versus Vbias for a 900 MHz input sinusoidal signal with amplitude of 1 V.

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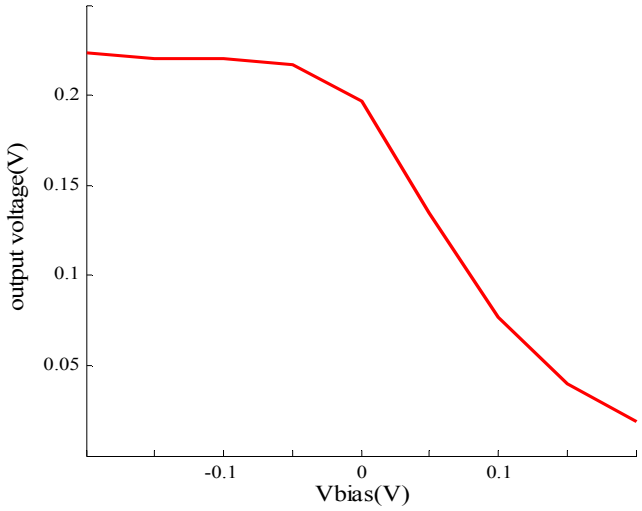

Figure 6. Output DC voltage of Villard voltage doubler versus Vbias for a 900 MHz input sinusoidal signal with an amplitude of 200 mV .

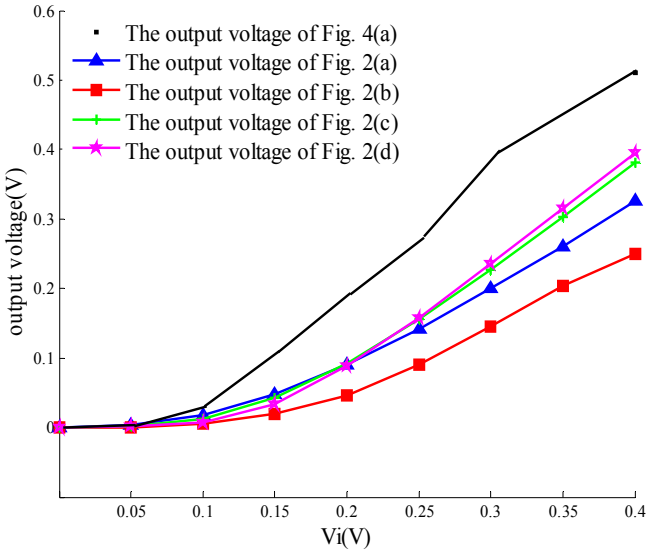

Figure 7. Comparing the output voltages of various configurations of Villard voltage doubler versus input signal amplitude up to 400 mV.

In PMOS version of conventional voltage doubler, at large voltage amplitudes, the drain-bulk junction diode of PMOS devices turns on due to high over drop voltages and thus the output voltage substantially drops. The proposed structure avoids this problem significantly increasing the output voltage. In the proposed design, the size of devices is also of great importance. The designed parameters for the rectifiers are listed in Table I. The size of PMOS devices are 2.5 times greater than the NMOS devices in the same position for better performance.

IV. Concolusion

In this paper we proposed a method for optimizing the Villard voltage multiplier resulting in enhanced output voltage in comparison with conventional counterparts. It is shown that

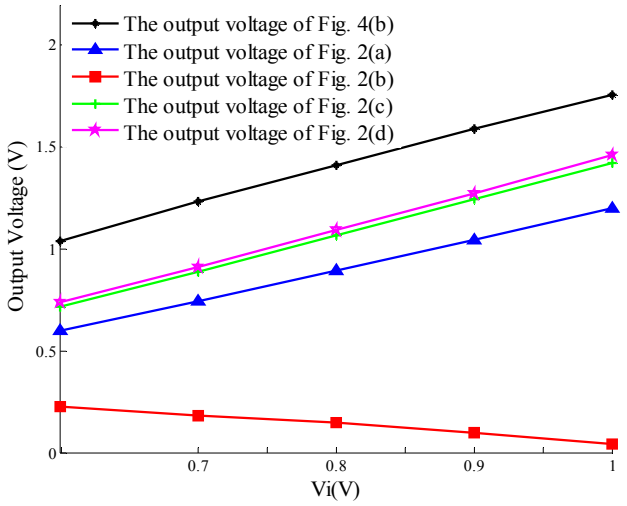

Figure 8. Comparing the output voltages of various configurations of Villard voltage doubler versus input signal amplitude from 600 mV up to 1 V.

TABLE I. Designed parameters for the Villard Voltage Doubler

Devices	Sizing of Transistors and Capacitors
MN1: (*W/L*) –Fingers –Multiplier	25 μm /0.18 μm – 35 –1
MN2: (*W/L*) –Fingers –Multiplier	20 μm /0.18 μm – 35 –1
MP1: (*W/L*) –Fingers –Multiplier	12.5 μm /0.18 µm – 35 –5
MP2: (*W/L*) –Fingers –Multiplier	25 μm /0.18 μm – 35 –2
MP3: (*W/L*) –Fingers –Multiplier	20 μm /0.18 μm – 5 –1
C_{out}	20 pF

a pre-biasing technique using a negative voltage is preferred for weak input signal amplitudes. The technique is implemented by using a half-wave rectifier in order to create a negative voltage from negative half cycles of the received input RF power in order to bias the gate of rectifying devices. With both negative and positive pre-bias voltages the output voltage improves depending on the input RF power level.

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