Processing Power Estimation of Simple Wireless Sensor Network Nodes by Power macro-modeling

M. Rafiee, M. B. Ghaznavi-Ghoushchi, B. Seyfe
Electrical engineering dept.
Shahed university
Tehran, IRAN
{rafiee, Ghaznavi, seyfe}@shahed.ac.ir

***Abstract*— The operation of wireless sensor networks is fundamentally constrained by available energy sources. In this paper, we propose a numerical power estimation technique for register transfer level. This technique allows estimating the power dissipation of components in WSN[1] to their statistical knowledge of primary inputs/outputs. During power estimation procedure, the sequence of an input stream is generated using input metrics and numerical macro-model function is used to construct a set of functions that maps the input metrics of a module to its output metrics. Then, simulation is performed and power dissipation is predicted by a macro-model function. The results are effective and highly correlated, with average error of 3.5%.**

Keywords-component; Wireless Sensor Networks, Processing Power, Macro-modeling

I. INTRODUCTION

Networked sensor systems are seen by observers as an important technology that will experience major deployment in next few years for a plethora of applications. Typical applications include, but are not limited to, data collection, monitoring, surveillance, and medical telemetry [1-2]. Wireless Sensor Network consists of large number of sensor nodes. These tiny nodes consist of sensing, data processing, and communicating components. Sensor Network (SN) aims to provide an efficient and effective connection between the physical and computational worlds. Sensor-nets are enabling previously impossible applications but since they are often battery-powered -typically by a pair of AA alkaline batteries that can supply 3 volts at 2000mAhr – sensor-net operations are fundamentally constrained by energy availability.

The four main ways in which nodes consume energy are sensing, communication, computation, and storage [3-6]. Energy constraints, coupled with the need for longer life-times, have led to a variety of techniques for modeling [7] and managing energy consumption.

Power estimation at RT level is crucial in achieving a short design cycle. Macro-modeling is the major technique for power estimation at RT-level.

The standard hierarchical simulation approach to RT-level power estimation consists of three steps: 1) functionally simulate the RT-level description and collect the input sequences for each circuit block. 2) Simulate each block at gate or circuit-level using the collected input sequences. 3) Add the power consumption for all blocks to produce the power consumption of the whole circuit. The disadvantage of this approach is that it requires the interaction between RT-level simulators and low-level simulators; power evaluation is actually done at gate-level.

Other technique for power estimation at RTL-level is macro-modeling. In this technique, low-level simulations of modules under their respective input sequence are replaced by power macro-model equation evaluation.

Macro-modeling techniques use capacitance models for circuit modules and activity profiles for data or control signals [8-10].

In this paper, we focus on the problem of power estimation at register transfer level (RTL) for processor components of node in sensor network.

Various power estimation techniques can be divided into two categories: probabilistic and statistical.

Probabilistic techniques [11-13] use the probabilities of the input stream and their propagation into the circuit to estimate the internal switching activities. These techniques are very efficient, but they cannot accurately capture factors like glitch generation and propagation. In statistical techniques [14-16] the circuit is simulated under randomly generated input patterns and the power dissipation is monitored using a power estimator. Therefore, the power values are used to estimate the power dissipation for every input stream.

The used technique generates random input vectors and its power dissipation is estimated using power estimator. The sequence vectors were provided to estimate power dissipation of a given circuit with certain statistical constraints such as confidence levels and error. The average power dissipation was estimated by simulating the circuit using a large number of samples in these vectors.

The input/output (I/O) metrics of our macro-model are the average input signal probability Pin, average input transition density Din, input spatial correlation Sin, average output signal probability Pout, average output transition density Dout, and output spatial correlation Sout.

The rest of this paper is organized as follows. In Section II we give the background for the input parameters of our macro-model. In Section III, we describe structure of WSN. In Section IV, we discuss about our macro-model

[1] Wireless sensor network

978-0-7695-3521-0/09 $25.00 © 2009 IEEE
DOI 10.1109/ICCET.2009.91

construction. This macro-model is evaluated in Section V. The results depict in Section VI. Section VII summarizes our work.

II. POWER MACROMODELING

Our macro-model consists of a nonlinear function and estimates the average power dissipation P_{avg} using equation (1).

$$P_{avg} = f(P_{in}, D_{in}, S_{in}) \quad (1)$$

The macro-model function $f(.)$ is obtained by a given module macro-modeling which maps space of input signal properties to the power dissipation of a circuit.

Given a circuit block with n inputs and a binary input stream $I=\{(i_{11},i_{12},\ldots,i_{1n})\},\ldots,(i_{l1},i_{l2},\ldots,i_{ln})\}$ of length l, these metrics are defined as follows:

$$P_{in} = \frac{\sum_{j=1}^{n}\sum_{k=1}^{l} i_{kj}}{n \times l} \quad (2)$$

$$D_{in} = \frac{\sum_{j=1}^{n}\sum_{k=1}^{l-1} i_{kj} \oplus i_{k+1\,j}}{n \times (l-1)} \quad (3)$$

$$S_{in} = \frac{\sum_{j=1}^{n}\sum_{k=1}^{n}\sum_{n=1}^{l} i_{nk} \oplus i_{nj}}{l \times n \times (n-1)} \quad (4)$$

The output metrics are the average output signal probability P_{out}, average output transition density D_{out} and output spatial correlation S_{out}. The macro-model function f in equation (1) can be used to construct to a set of functions f_A , f_B and f_C that maps the input metrics of a macro-block to its output metrics P_{out}, D_{out}, S_{out} are derived in equations (5), (6), and (7):

$$P_{out} = f_A(P_{in}, D_{in}, S_{in}) \quad (5)$$

$$D_{out} = f_A(P_{in}, D_{in}, S_{in}) \quad (6)$$

$$S_{out} = f_A(P_{in}, D_{in}, S_{in}) \quad (7)$$

The sequence of an input stream is generated for a desired input metrics, then the output stream sequence is extracted by the output waveforms simulation technique, and the power dissipation is predicted by macro-model function.

III. STRUCTURE OF WSN

A sensor network is modeled as a set of heterogeneous entities. Sensor nodes deployed over the area of interest. They are triggered by a certain set of stimuli that are transmitted to a remote base-station. Three main types of sensor nodes need to be created and supported: 1) target nodes that do stimulation of the sensors, 2) sensor nodes that monitor events and 3) user nodes that query the sensors and are the final destination of the target reports.

Node performs a simple task: take an analog sample, and transmit the data over the wireless link to one or more receivers. Node module functionally consists of three concurrent modules, which are analogous to the four main components of the node, namely, Analog-To-Digital (ADC) Converter, Microcontroller, Encryption and Transceiver.

The ADC converts the analog signal into digital values. Transceiver Sender receives data from sensor module, or receives data from other node module or transmits the data to other node module through the wireless channel. Microcontroller controls the whole process by setting an interface between the two other sections.

All the nodes perform the same function but at different frequency, data resolutions and data domains.

ADC converts the analog value into 10-bit digitals. Module μC takes the data from the ADC, adds the address of the receiver node and provides the data payload for the Transceiver module. Transceiver can send data to next node or sink by using IEEE 802.15.4 standard [17] (CSMA/CA policy).

Sink consists of two components, Receivers, and CPU. Receiver receives data from concurrent node module and sends to CPU Module.

Fig. 1 shows the overall structure of sample WSN system. Fig. 2 depicts the structure of Node module in WSN.

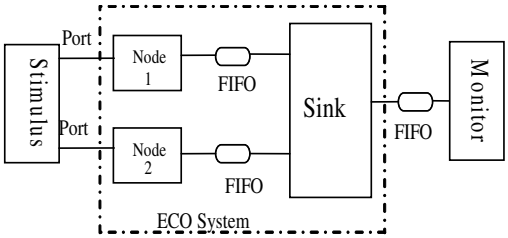

Figure 1. Overall eco system

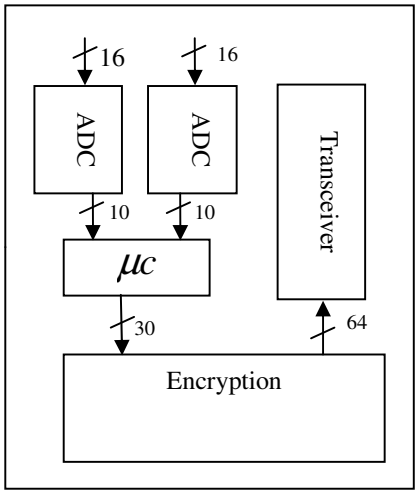

Figure 2. Node module

IV. MACROMODEL CONSTRUCTION

Several methods [18-20] have been proposed to construct power macro-modeling.

In used static power estimation procedure, the input metrics is computed for an input stream. The output stream sequence is derived from the output waveforms of each module. The average power dissipation P_{avg} is predicted using equation (1).

We define a power macro-model as a linear function for the estimation of power dissipation.

$$P_{avg} = \beta_0 + \beta_1 P_{in} + \beta_2 D_{in} + \beta_3 S_{in} \quad (8)$$

Where the coefficients β_i are the unknown and are to be determined during the characterization using regression analysis as discussed in [21]. To improve accuracy, another option is the function considering I/O statistics P_{in}, D_{in}, S_{in}, P_{out}, D_{out}, and S_{out} as independent variables in (9):

$$P_{avg} = \beta_0 + \beta_1 P_{in} + \beta_2 D_{in} + \beta_3 S_{in} + \beta_4 P_{out} + \beta_5 D_{out} + \beta_6 S_{out} \quad (9)$$

The key difference between the (8), (9) models is the number of fitting coefficients that impact the achievable accuracy and the characterization effort.

V. MODEL ACCURACY ANALYSIS

Power macro-model is built at RTL level. The accuracy of the proposed model is evaluated on processor components of wireless sensor network. For those modules, we generated random values of P_{in}, D_{in}, and S_{in}. The function f in equation (1) is used to construct to a set of functions f_A, f_B and f_C that maps the input metrics of a module to its output metrics P_{out}, D_{out}, S_{out}.

The power values predicted by macro-model are compared with those from simulations, and average errors are computed.

Experimental results show that our randomly generated sequences are with accurate statistics and highly convergence. We generated 40 sequences with 10, 16, 64 bits wide. The sequence length is 200 vectors for the modules

VI. RESULTS

It is obvious from Table I that the function is accurate for estimating the average power for ADC, Microcontroller, and DES modules. In Table I the first column represents the name of modules. Column two give the average error for the estimates obtained with our macro-model. Reference values for the module's power dissipation are obtained using time delays from the Synopsys PowerCompiler. In our experiments, the average error is 3.5%.

TABLE I. ACCURACY OF POWER ESTIMATION

Circuits	Average error %
ADC-1	7.2
ADC-2	4
ADC-3	8
ADC-4	3
ADC-5	9.6
ADC-6	5.1
DES-1	0.59
DES-2	0.33
DES-3	0.17
DES-4	0.44
DES-5	0.29

Power consumption used model of microcontroller is less than 0.0001 mW hence effect of this power in total processing power is inconsiderable.

Fig. 3 illustrates power comparison between macro-model and reference simulated power in ADC module.

Fig. 4 depicts power comparison between macro-model and reference simulated power in DES module.

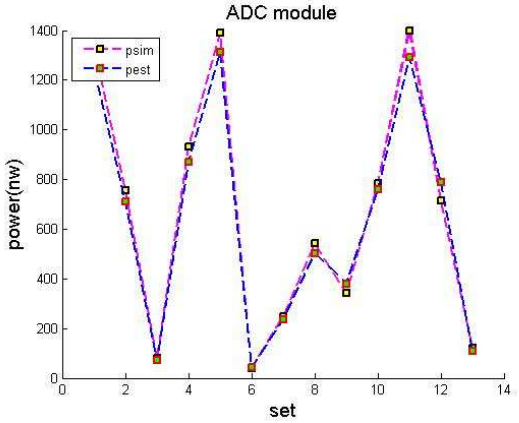

Figure 3. Power comparison between macro-model and reference simulated power in ADC module

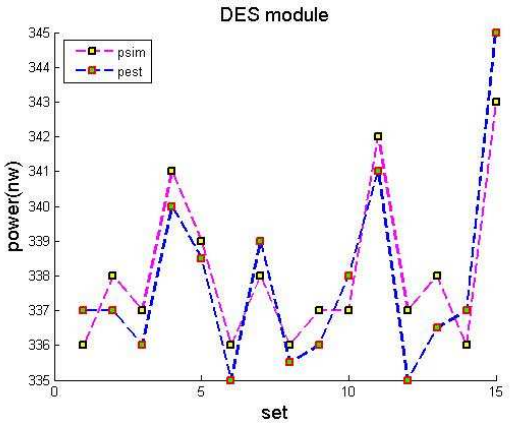

Figure 4. Power comparison between macro-model and reference simulated power in DES module

VII. CONCLUSIONS

Sensor-net lifetime is severely constrained by the available energy source, Hence in this paper we present a new numerical macro-modeling technique for high level power estimation. This procedure uses input/output (I/O) statistical parameters at the architectural level. We compare our macro-modeling results with Synopsys Power Compiler power estimation tool and find accuracy of this technique is good. Our model shows average error of 3.5%.

REFERENCES

[1] I.F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci, "Wireless sensor networks: a survey",Computer Networks, 38(4), pp. 393–422, March 2002.

[2] D. Estrin, L. Girod, G. Pottie, and M. Srivastava, "Incrementing the World with Wireless Sensor Networks", IEEE ICASSP 2001, 4, pp. 2033-2036, 2001.

[3] L. Doherty,B. Warneke,B. Boser, and K. Pister, " Energy and performance considerations for smart dust", International Journal of Parallel Distributed Systems and Networks, vol. 4, no. 3, pp. 121-133, 2001.

[4] P. Dutta, M. Grimmer, A. Arora, S. Bibyk, and D. Culler, "Design of a wireless sensor network platform for detecting rare, random, and ephemeral events", in Proceedings of the Fourth International Conference on Information Processing in Sensor Networks (IPSN '05).

[5] S. Madden, " The design and evaluation of a query processing architecture for sensor networks", Ph.D. dissertation, U.C.Berkeley, 2003.

[6] J. Polastre, "Design and implementation of wireless sensor networks for habitat monitoring", Master's thesis, University of California at Berkeley, 2003.

[7] V. Shnayder, M. Hempstead, B. rong Chen, G. Werner-Allen, and M. Welsh, "Simulating the power consumption of large-scale sensor networkapplications", in Proceedings of the Second ACM Conference on Embedded Networked Sensor Systems (SenSys'04), Nov. 2004.

[8] S. Powell and P. Chau, "Esitmating power dissipation of VLSI signal processing chips: The PFA techniques", Proceeedings of IEEE Workshop on VLSI Signal Processing IV, vol. IV, pp.250-259, 1990.

[9] P.Landman and J. Rabaey, "Power esitmation for high-level synthesis", Proceedings of IEEE European Design Automation Conference, pp.361-366, Feb, 1993.

[10] D. Liu and C. Svensoon, "Power consumption estimation in CMOS VLSI chips", IEEE Journal of Solid State Circuits, vol. 29, pp.663-670, Jun. 1994.

[11] A. A. Ghose, S. Devdas, K. Keutzer and J. White, "Estimation of average switching activity in combinational and sequential circuits," In Proceedings of the 29th Design Automation Conference, pages 253-259, June 1992.

[12] F. N. Najm, R. Burch, P. Yang, and I. N. Hajj, "Probabilistic simulation for reliability analysis of CMOS circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 9(4):439-450, April 1990.

[13] R.Marculescu, D. Marculescu, and M. Pedram, "Logic level power estimation considering spatiotemporal correlations," In Proceedings of the IEEE International Conference on Computer Aided Design, pages 224-228, November 1994.

[14] G.Y. Yacoub and W.H.Ku, "An accurate simulation technique for short-circuit power dissipation," In Proceedings of International Symposium on Circuits and Systems, pages 1157-1161, 1989.

[15] C. M. Huizer, "Power dissipation analysis of CMOS VLSI circuits by means of switch-level simulation," In IEEE European Solid State Circuits Conf., pages 61-64, 1990.

[16] C. Deng. "Power analysis for CMOS/BiCMOS circuits," In Proceedings of 1994 International Workshop on Low Power Design, pages 3-8, April 1994.

[17] L. Cheng, "IEEE 802.15.4 MAC Protocol Study and Improvement", A Dissertation Submitted in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, Georgia State University, 2000.

[18] G. Bernacchia, and M. C. Papaefthymiou, "Analytical Macromodeling for High-Level Power Estimation", In Proc. IEEE Int. Conf. Computer Aided Design, pp.280-283, 1999.

[19] M. Anton, I. Colonescu, E. Macii, and M. Poncino, "Fast characterization of RTL power macromodels", In IEEE Proc. of ICECS, pp. 1591–1594, 2001.

[20] S. Gupta and F.N. Najm, "Power Macromodeling for High Level Power Estimation," In Proceeding IEEE Transactions on VLSI, 1999.

[21] Q. Qiu, Q. Wu, M. Pedram, C. S. Ding, "Cycle-Accurate Macro-Models for RT-Level Power Analysis", International Symposium on Low Power Electronics and Design, pp. 125 – 130, 18-20 Aug 1997.