17th ICEE 2009
Iranian Conference on Electrical Engineering
www.icee.ir/2009
IUST

Algorithmic Design of CMOS Miller Op-Amps

A.A. Bagheri-Soulla*, M.B. Ghaznavi-Ghoushchi **
*School of Engineering, Shahed University, Tehran, IRAN, ali.soulla@gmail.com
** School of Engineering, Shahed University, Tehran, IRAN, ghaznavi AT shahed.ac.ir

Abstract: *In This paper we present an algorithmic approach for design of CMOS Miller Op-Amps. The proposed approach is based on EKV and BSIM transistor models. The design of an Op-Amp starts with an acceptable error based on hand calculated formulation. Due to the various lacks of using optimization algorithms, this approach does not based on optimization techniques. The target design technology is 0.5um with parameters of level 49. We provide a C++ based tool that can design target Miller Op-Amp. There are 5 user defined design parameters including gain, phase margin, unity gain bandwidth, power and slew rate. User can feed program by point value for above parameters or define range for gain, phase margin and unity gain bandwidth. In both of design approaches user can force program to try to minimize the power. Therefore this tool may be used for low-power Miller Op-Amp design too. In ranged parameter approach user should specify which design is better between acceptable designs provided by the toolset. Program provides a spice net list as output if design's specifications confirmed by HSPICE.*

Keywords: Miller Op-Amp**,** Op-Amp design, Automatic analog design, EKV model, BSIM model.

1. Introduction

Automatic analog design is one of the interesting topics in analog design. It is about 30 years that some one attempted to automate analog design process.

Many Computer-Aid Design (CAD) tools [1–9] have been developed for analog circuit synthesis, especially for Op-Amp synthesis. The major problem in CMOS analog and digital design is the transistor sizing to meet the desired specs. In circuit sizing, three essential issues, which are accuracy, global optimality and computation time, have to be properly addressed in the design of practical analog synthesis CAD tools.

Equation-based approaches [2–5] rely heavily on simplifications of circuit equations and device models. Using special optimization techniques for equations, such as geometric programming in [2], these tools can solve the optimization problem in minutes but they suffer from an important lack. These optimization techniques force equations to be in specific form, but we can not write all of the target equations by that limitation. So we have to simplify our equations and some time we can not encounter very important factors in our model, so that we do an optimization on a virtual model of system rather than an actual/real model.

Simulation-based approaches [6-8] resolve the accuracy problem by directly using SPICE for circuit evaluation. Tools, like DELIGHT.SPICE in [6], use gradient-based optimization techniques, which makes them capable of finding only local optimal solutions. In order to find the global optimum for circuits, simulated annealing (SA) is used in [7] and [8]. As introduced in [10], in theory, with sufficiently large annealing times, SA is able to find the global optimum within the design space, regardless of the initial condition. However, the design space is usually rather complicated for most real design problems. It is difficult to design an adaptation process for plain SA, without any knowledge of the circuit, to settle to the exact global optimum, which leads to the pessimistic assertion in [2] about SA. In order to increase the chance of reaching the global optimum, long annealing runs are used by these CAD tools. In a simple Op-Amp design we have about 18 design parameter that made very broad design space.

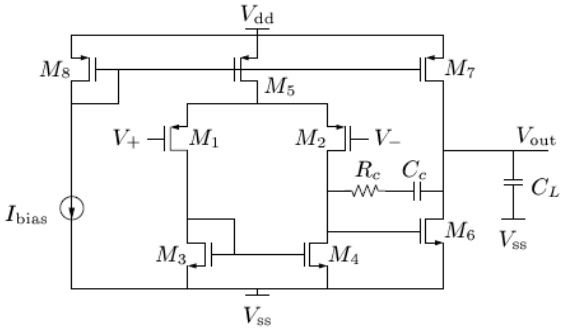

Fig. 1: Two stage Miller Op-Amp [2].

In this paper we will design miller Op-Amp illustrated in figure 1. Here we do not try to optimize circuit's equations. Our approach designs a miller Op-Amp algorithmically. We try to achieve user's entered point value. If user enters range for design parameter we can search that ranges and propose best design for user and we can try to minimize the power on user request. For this purpose we developed a C++ based toolset. Output of the software will be checked by HSPICE before inform to user. There can be two kind of fault in design process 1-entered constrains made infeasibility in equations and 2-design is done by solver but difference of desired value

with HSPICE result is more than margins that defined. In this step we can not predicate about feasibly of entered value. Design's technology is 0.5um on real MOSIS [13] level 49 test parameters.

The remainder of this paper is organized in the following manner: In second part of this paper we described target Op-Amp structure and relations between design parameters. In section 3 we presented algorithm for point value design followed by Ranged Value design. Section 4 comes with design examples resulted from our tool and their HSPICE simulation results. Finally section 5 concludes the paper.

2. Circuit Fundamentals

Figure 1 illustrates the target miller Op-Amp. In this topology, we have an Op-map whit PMOS input. C_L is load capacitor, C_C and R_C are compensation capacitor and resistor respectively. I_{bias} is the bias current source.

2.1 Design Parameters Equations

Here we will bring gain, phase margin, unity gain bandwidth, power, and slew rate equations. The following design equations and specs must be met simultaneously driving a given load capacitor. The total current for the amplifier must be less than (*power/Vdd*) counting the bias current, flowing through M8.

Equation (1) is gain equation; we have two gain stages and each term refer to one of them.

$$A_V = A_{V1} \times A_{V2} = \left(\frac{g_{m2}}{g_{ds2} + g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right) \quad (1)$$

Equation (2) is for unity gain bandwidth.

$$\omega_u = \frac{g_{m2}}{C_C} \quad (2)$$

With the 4-pole approximation, the phase margin (PM) equation can be written as (3).

$$PM = 180^o - \tan^{-1}\frac{\omega_u}{|p_1|} - \tan^{-1}\frac{\omega_u}{|p_2|} - \tan^{-1}\frac{\omega_u}{|p_3|} - \tan^{-1}\frac{\omega_u}{|p_4|} \quad (3)$$

Poles relation shows in equation set (4) where C_g is all MOS capacitances from the gate to AC ground.

$$\begin{cases} |p_1| \cong \dfrac{g_{m2}}{A_v C_C} \\ |p_2| \cong \dfrac{g_{m6}}{C_L} \\ |p_3| \cong \dfrac{1}{R_C C_1} \simeq \dfrac{g_{m6}}{C_{g6}} \\ |p_4| \cong \dfrac{g_{m3}}{C_{g3} + C_{g4}} \\ C_1 \cong C_{g6} + C_{db2} + C_{db4} \end{cases} \quad (4)$$

Initially, there is no a prior knowledge on whether p3 or p4 is the actual lower frequency pole. Now we will treat on equation (3), $\frac{\omega_u}{|p_1|} = A_v$ which is a very large number. The *arctan* of a very large number is approximately 90^o. Also we want to design the amplifier so that it has a 2-pole-like settling which will require that the magnitude of the third pole be $|p_3| \geq 10\omega_u$ and fourth pole be $|p_4| \geq 20\omega_u$. Substituting *arctan(0.1)=5.71*^{o} and *arctan(0.2)=2.86*^{o}, so the total phase shift from these 2 non-dominate poles is 8.57^o. Now the phase margin in equation (3) becomes:

$$PM = 81.43^o - \tan^{-1}\frac{\omega_u}{|p_2|} \quad (5)$$

Power of Op-Amp is in equation (6) and slew rate's equation set is (7), in normal condition we need input slew rate be smaller than output one.

$$P = V_{dd} \times (I_{bias} + I_5 + I_7) \quad (6)$$

$$\begin{cases} SR_{input} = \dfrac{I_5}{C_C} = \dfrac{2I_2\omega_u}{g_{m2}} \\ SR_{output} = \dfrac{I_7}{C_L + C_C} > SR_{input} \end{cases} \quad (7)$$

2.2 Design Parameters and Their Relations

In this section design parameters and equations are related to transistor parameters which lead to transistor sizing.

We start at first by phase margin. From equations (3) and (5) we can extract equation (8).

$$g_{m6} = \frac{1}{\tan(81.43 - PM)}\omega_u C_L \quad (8)$$

From power equation beside slew rate equation current of M5 and M7 can be calculated as equation (9) there is a free parameter that none of our equation made any force on that. We took C_C as free parameter.

$$\begin{cases} \dfrac{I_7}{I_5} \geq 1 + \left(\dfrac{C_L}{C_C}\right) \\ I_7 + I_5 = \dfrac{P}{V_{dd}} - I_{bias} \end{cases} \quad (9)$$

From slew rate equation beside equation (5) we can write equation (10).

$$\frac{g_{m6}}{g_{m2}} \geq \frac{1}{\tan(81.43 - PM)} \times \frac{C_L}{C_C} \quad . \quad (10)$$

From EKV model we can re-write inversion factor as (11) where n is slope factor and V_t is thermal voltage [12]. Inversion factor relation to V_G is in (12) [12].

$$i_F = \left(\frac{I_{ds}}{g_m n V_t - 0.5}\right)^2 - \frac{1}{4} \quad . \tag{11}$$

$$\begin{cases} i_F = \ln^2\left[1+\exp\left(\frac{V_p - V_S}{2V_t}\right)\right] \\ V_p = \frac{V_G - V_{th}}{n} \end{cases} \tag{12}$$

Above equations relate DC parameters like current and voltage to the transistor AC parameters.

If we were in digital space our transistor's channel length can be token constant, but in analog design, channel length's effect is more important from channel width. In this work we first calculate channel length and channel width is a function of channel length (13).

$$W = \frac{I_{Dsat}}{2nK_p V_t^{\,2} . i_F} . L \quad . \tag{13}$$

There is an important note about relation of g_{ds} to early voltage and length of transistor channel. In equation set (14) we show this relation [11].

$$\begin{cases} r_o = \frac{1}{g_{ds}} = \alpha\left(\frac{V_a + V_{th} + V_{gt}}{I_{Dsat}}\right) \\ V_a = \varepsilon_{sat} . L \\ \varepsilon_{sat} = \frac{2V_{sat}}{\mu(V_{gt})} \\ V_{gt} = V_{gs} - V_{th} \end{cases} \quad . \tag{14}$$

Where α will be 0.5 when Vgt is low value and Vsat is drain source saturation voltage and defined in EKV model as (15) [11].

$$V_{DSsat} = V_t . (2\sqrt{i_F} + 4) \quad . \tag{15}$$

On the other hand we have $\mu(V_{gt})$. This parameter is mobility and figure 2 illustrate its relation to Vgt for a sample device, and its equation is (16) [11].

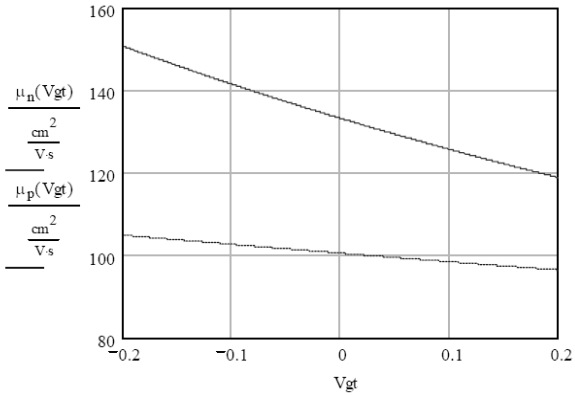

Fig. 2: mobility relation to V_{gt} [11]

$$\mu_{n,p}(V_{gt}) = \frac{U0_{n,p}}{1 + UA_{n,p} . \frac{V_{gt} + 2.\left|V_{th0n,p}\right|}{TOX} \ldots} \tag{16}$$

$$\ldots \frac{}{+ UB_{n,p} . \left(\frac{V_{gt} + 2.\left|V_{th0n,p}\right|}{TOX}\right)^2}$$

Where U0, UA, UB are level 49 parameters and TOX is oxide thickness.

3. Proposed Design Algorithm

In this section our design algorithm is described. Our proposed algorithm accepts two different user specified constraints, exact point value specs and Ranged Value specs. At the first step point value design is described and then it is expanded to range value parameter design and power minimization step is finally introduced.

3.1 Point value design

In this algorithm we set some parameter by our knowledge about circuit these are W8 (M8 channel width), Ibias (bias current source value), C_C (compensation capacitor), V_{G2} (bias voltage of transistors M1, M2). All the other circuit's parameters should be set by algorithm.

First we find I_5, I_7 by means of (9) after that we will calculate g_{m6} (8) and from (10) we calculate g_{m2}. Now we have I_5 and g_{m2} from these parameters we have i_{F2} and then we can achieve to V_{S2} because we know V_{G2}. Now we have V_{gt2} so that μ_{p2} can be found so that we have $\varepsilon_{sat\,2}$. We can do a routine like above for M6. If we solve M6 equations we have VG6 and because of circuit conditions VG4=VG6 so that $\varepsilon_{sat\,4} = \varepsilon_{sat\,6}$.

Again by means of our knowledge we know in a two stage Op-Amp first stage's gain can be lower than second stage so that we set a parameter to divide gain between stages.

Using gain relation of first stage $\left(\frac{g_{m2}}{g_{ds2} + g_{ds4}}\right)$ we were calculate g_{m2} initially, so we know $g_{ds2}+g_{ds4}$. Here we have a complicated formulation for this equation. We calculate all of the parameters before except L2 and L4 as the channel length of M2 and M4 respectively. For this purpose we developed an approach that can calculate these parameters beside in a loop whit some conditions to achieve $g_{ds2}+g_{ds4}$.

Now because of circuit conditions and alike current mirror condition between M3, M4 and M6, we will chose L6=L4.

Then we focused on second gain stage with the given $\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right)$ as the second stage gain in this equation, we know g_{m6} and g_{ds6} so we need to calculate g_{ds7}. We

know W7 and current of M7 that is I_7. We should combine our equations (12), (14), (15), (16) to yield an equation between r_{o7} and V_{gt7}. The variation of r_{o7} vs. V_{gt7} is depicted in figure 3. We will find V_{gt7} by numerical techniques. By means of equation set (14) we can calculate L7. We know M5, M7 and M8 are in current mirror form so we took L8=L5=L7.

Finally we used equation (13) to find W6, W4 and W2. Since (M1, M2) and (M3, M4) are differential pairs we may have (L1=L2, W1=W2) and (L3=L4, W3=W4). And using (4) we set $R_C = \frac{1}{g_{m6}}$.

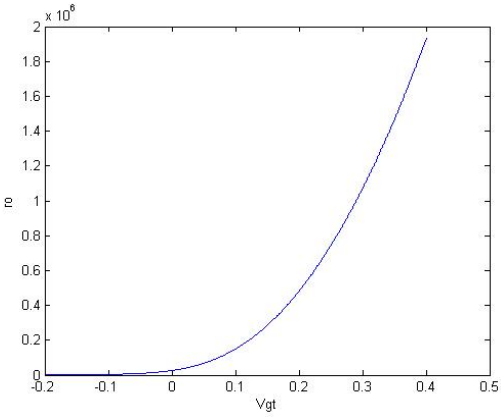

Fig. 3:r_{o7} vs. V_{gt7}

3.2 Ranged Value Design

In previous step we explain completely design algorithm for a point value problem. If user specifies ranges for its specs, our developed toolkit starts to design and examine circuit for all combinations in a predefined set of points in each range. Number of design that should be done is S^R. Where S is number of sample from each range and R is the number of range parameters.

Upon completion of each point value design, the results are compared with HSPICE simulation results to evaluate the design. Finally software can propose best net list by means of user direct on major restrictions (higher gain, higher phase margin, higher gain bandwidth or mixed of them).

It is possible to decrease power of final net-list as predestined. For this purpose we will decrease desired power step by step. We do this action until designed system confirmed.

Figure 4-6 illustrate point value Design, Ranged Value Design, and power minimization Algorithm.

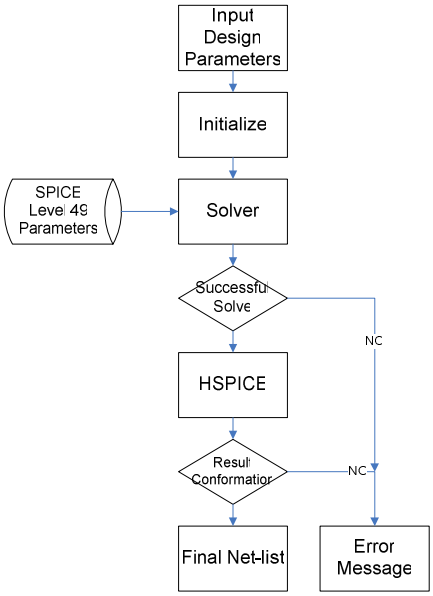

Fig. 4: point value design algorithm

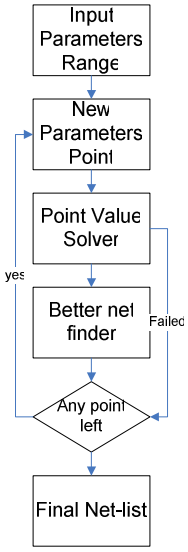

Fig. 5: Ranged Value design algorithm

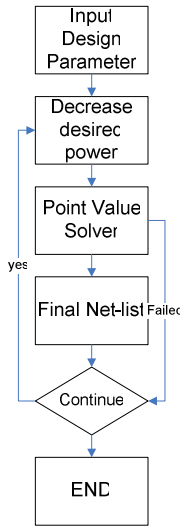

Fig. 6: power minimization algorithm

4. Design samples

In this section some experimental results of applying the developed tool set is presented. There are 4 design set. In 4.1 we do point value design table I. In 4.2 we have two kind of design set, table III is Ranged Value design in which one of parameters was design target and table V shows a Ranged Value design, that target parameters order importance is available. Finally in table VII we redo the design of table V with power minimization request.

4.1 Point value design

Here we have two point value designs. Table I contains design parameters and simulation result of HSPICE for designed circuit.

TABLE I: Point Value design parameters

Design parameters	Set 1		
	desired	HSPICE	Error
Gain (db)	90	89.39	0.67%
PM (Deg)	60	60.65	1.08%
GB (MHz)	6	6.375	6.25%
Power (uW)	500	507.17	1.43%
	Set 2		
Gain (db)	85	84.01	1.16%
PM (Deg)	70	68.97	1.47%
GB (MHz)	4	4.071	1.77%
Power (uW)	400	401.68	0.42%

TABLE II: Point Value design 'I' net list parameters

Parameter	Set 1		Set 2	
	W (um)	L(um)	W(um)	L(um)
M1	55.11754	2.672980	24.78690	2.273985
M2	55.11754	2.672980	24.78690	2.273985
M3	17.79724	2.471980	56.65871	2.072984
M4	17.79724	2.471980	56.65871	2.072984
M5	17.40741	5.203485	13.70370	2.124504
M6	124.5807	2.471980	396.6110	2.072984
M7	60.92593	5.203485	47.96296	2.124504
M8	5.000000	5.203485	5.000000	2.124504
	Value		Value	
Ibias	10 uA		10 uA	
Cc	4 pF		4 pF	
Rc	937.7305 ohm		663.6918 ohm	
CL	10 pF		10 pF	

4.2 Ranged Value design

In this part we want to show the ability of program to find better net list for Ranged Value design by user's requirements.

In table III and V "number of design" shows S^R that was explained in 3.2. "Successful ratio" indicates how many of designs were successful and "design target" is request in network selection phase.

TABLE III: Ranged Value design parameters

Design parameters	Set 1		Set 2	
	desired	HSPICE	desired	HSPICE
Gain (db)	85-90	84.709	80-90	80.424
PM (Deg)	55-65	66.586	50-70	70.280
GB (MHz)	5-7	6.6748	4-7	7.0029
Power (uW)	500	508.48	500	510.60
Number of design	64		125	
Success ratio	62.5%		56.8%	
Design target	Max PM		Max GB	

TABLE IV: Ranged Value design 'III' net list parameters

Parameter	Set 1		Set 2	
	W (um)	L(um)	W(um)	L(um)
M1	39.91824	1.938988	28.92482	1.404994
M2	39.91824	1.938988	28.92482	1.404994
M3	27.77537	1.737988	19.24143	1.203994
M4	27.77537	1.737988	19.24143	1.203994
M5	17.40741	2.746168	17.40741	1.938535
M6	194.4276	1.737988	134.6900	1.203994
M7	60.9259	2.746168	60.92593	1.938535
M8	5.000000	2.746168	5.000000	1.938535
	Value		Value	
Ibias	10 uA		10 uA	
Cc	4 pF		4 pF	
Rc	684.5107 ohm		684.5107 ohm	
CL	10 pF		10 pF	

We can support design target importance. Table V illustrate this ability. In this table design target row contains importance of design targets respectively. For example in design set 1 we need an Op-Amp with higher phase margin but maybe we have some net-list with same phase margin here net-list selector should select design with higher gain between those designs.

TABLE V: Ranged Value design parameters with target order

Design parameters	Set 1		Set 2	
	desired	HSPICE	Desired	HSPICE
Gain (db)	80-90	81.305	80-90	89.187
PM (Deg)	50-70	70.511	50-70	58.417
GB (MHz)	4-7	4.1811	4-7	7.2155
Power (uW)	500	508.15	500	507.64
Number of design	125		64	
Success ratio	72%		64.06%	
Design target	1- Max PM 2- Max gain		1- Max GB 2- Max gain	

TABLE VI: Ranged Value design 'V' net list parameters

Parameter	Set 1		Set 2	
	W (um)	L(um)	W(um)	L(um)
M1	17.90789	1.930988	63.65820	2.435983
M2	17.90789	1.930988	63.65820	2.435983
M3	9.855338	1.729988	13.40285	2.235983
M4	9.855338	1.729988	13.40285	2.235983
M5	17.40741	2.869987	17.40741	5.586496
M6	68.98737	1.729988	93.81992	2.235983
M7	60.9259	2.869987	60.92593	5.586496
M8	5.000000	2.869987	5.000000	5.586496
	Value		Value	
Ibias	10 uA		10 uA	
Cc	4 pF		4 pF	
Rc	1034.224 ohm		1012.254 ohm	
CL	10 pF		10 pF	

4.3 Ranged design with power minimization

Table VII is redesign of table V with power minimization aim.

TABLE VII: Power minimization of Table V

Design parameters	Set 1		Set 2	
	desired	HSPICE	desired	HSPICE
Gain (db)	80-90	79.229	80-90	89.045
PM (Deg)	50-70	69.818	50-70	57.834
GB (MHz)	4-7	5.3192	4-7	7.2745
Power (uW)	min	307.47	min	486.62
Number of designs	64		64	
Success ratio	64.06%		64.06%	
Design target	1- Max PM 2- Max gain		1- Max GB 2- Max gain	

TABLE VIII: power minimization result net list parameters

Parameter	Set 1		Set 2	
	W (um)	L(um)	W(um)	L(um)
M1	22.53706	1.192996	65.16405	2.336984
M2	22.53706	1.192996	65.16405	2.336984
M3	16.55689	0.991995	11.81720	2.135984
M4	16.55689	0.991995	11.81720	2.135984
M5	10.37038	1.601243	16.66667	5.667196
M6	115.8982	0.991995	82.72042	2.135984
M7	36.29632	1.601243	58.33333	5.667196
M8	5.000000	1.601243	5.000000	5.667196
	Value		Value	
Ibias	10 uA		10 uA	
Cc	4 pF		4 pF	
Rc	941.0417 ohm		1073.719 ohm	
CL	10 pF		10 pF	

5. Conclusion

In this paper we developed an algorithmic design approach for CMOS Miller Op-Amp. Our approach is based on EKV and BSIM3.3 (Level 49) models.

In spite of conventional approach of using equation-based models for optimization purpose, we used equation-based models for direct design of analog circuits. This is due to the various lacks of using equation-based modelling for optimization including: (a) all of the equations could not be feed to optimization tools (b) some of optimization tools can not support non linear boundary equations and so on.

We developed two different design methods for CMOS Miller Op-Amps: point value design and Ranged Value design. The user defined design specs are gain, phase margin, unity gain bandwidth, power and slew rate.

We developed a toolset based on C++ for the proposed methods. In the point value design, the output is a HSPICE net-list, and in Ranged Value design the output is a net-list that selected by means of user direct on major restrictions (higher gain, higher phase margin, higher gain bandwidth or mixed of them). In both of former design approaches power can be decreased if feasible.

The resulted designs are confirmed by HSPICE simulations, in acceptable error margin. In Ranged Value design, results are in user defined ranges and output net-list confirmed by HSPICE simulations, finally results of power reducing tool has acceptable validity.

References

[1] W. Kruiskamp and D. Leenaerts, "DARWIN: CMOS opamp synthesis by means of a genetic algorithm," in Proc. 32nd ACM/IEEE Design Automation Conf., 1995, pp. 433–439.

[2] M. del Mar Hershenson and S. Boyd, "GPCAD: A tool for CMOS Op-Amp synthesis," in Proc. IEEE/ACM Int. Conf. CAD, Nov. 1998, pp. 296–303.

[3] M. Degrauwe et al., "IDAC: An interactive design tool for analog CMOS circuits," IEEE J. Solid-State Circuits, vol. SC-22, no. 12, pp. 1106–1116, Dec. 1987.

[4] R. Harjani, R. Rutenbar, and L. Carley, "OASYS: A framework for analog circuit synthesis," IEEE Trans Computer Aided Des. Integr. Circuits Syst., vol. 8, no. 12, pp. 1247–1266, Dec. 1989.

[5] H. Koh, C. Sequin, and P. Gray, "OPASYN: A compiler for CMOS operational amplifiers," IEEE Trans Computer Aided Des. Integr. Circuits Syst., vol. 9, no. 2, pp. 113–125, Feb. 1990.

[6] W. Nye et al., "DELIGHT.SPICE: An optimization-based system for the design of integrated circuits," IEEE Trans Computer Aided Des. Integr. Circuits Syst., vol. 7, no. 4, pp. 501–518, Apr. 1988.

[7] E. Ochotta and L. Carley, "Synthesis of high-performance analog circuits in ASTRX/OBLX," IEEE Trans Computer Aided Des. Integr. Circuits Syst., vol. 15, no. 3, pp. 273–294, Mar. 1996.

[8] F. Medeiro et al., "A statistical optimization-based approach for automated sizing of analog cells," Proc. IEEE ICCAD, pp. 594–597, 1994.

[9] J. Yuan, N. Farhat and Jan Van der Spiegel, "GBOPCAD: A Synthesis Tool for High-Performance Gain-Boosted Opamp Design" IEEE transactions circuits and system I: regular papers vol.52, No.8, August 2005.

[10] R. Rutenbar, "Simulated annealing algorithms: An overview," IEEE Circuits Dev. Mag., vol. 5, no. 1, pp. 19–26, Jan. 1989.

[11] Willy M.C. Sansen, Analog Design Essentials, the Springer International Series in Engineering and Computer Science, Vol. 859 1st ed. 2006. 2nd printing, 2006.

[12] D. Stefanovic, M.Kayal, Structured Analog CMOS Design, Springer Science, 2008, pp.7-48

[13] http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ibm-05/t86d_5am_ni-params.txt