Parallel and Series Harmonic Resonance Prevention by Anti-Resonance Hybrid Capacitor System for Power Factor Correction

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***Abstract*—This paper discusses a simple control scheme for an anti-resonance hybrid power factor correction capacitor bank in low-voltage industrial power systems. Conventional power factor correction capacitors are prone to failure due to high voltage and current caused by parallel and series resonance with the system inductance. Load current harmonics and source voltage harmonics are causes of resonance when they match the system resonance frequency. Moreover, the system parameters are dynamically changed; therefore, harmonic resonance might occur even if it had been studied before the capacitor installation. Resonance current flowing through the capacitor, as well as through the power source can be damped by using an anti-resonance hybrid capacitor system. The main objective here is to suppress resonance current by applying a simple and effective control scheme to the hybrid power factor correction capacitor system. Simulation results verify the viability and effectiveness of the proposed system for reactive power compensation and any harmonic resonance elimination.**

Keywords-Anti-resonance system, Capacitor banks, Harmonics, Power factor, Resonance.

I. INTRODUCTION

Most loads used in industry power systems are inductive. In inductive loads current lags voltage, therefore, reactive power is absorbed from the mains and power factor is less than unity. The poor power factor has the following disadvantages:

- Losses in the distribution system are increased,
- Capacity of the transmission and distribution network is unnecessarily occupied, and
- Voltage regulation at the load bus is degraded. [1]

Power factor correction is, therefore, widely adopted for industrial loads. This is usually achieved by installing capacitor banks and, recently, by employing power semiconductor and static converter based compensators such as static VAR compensators (SVC), static condensers (ATATCON or STATCOM) and active power filters [2, 3]. However, power capacitors are the most economic solution among them [4]. Even though, capacitors do not generate harmonics, they can influence harmonic levels on the distribution systems. One of the most serious problems is harmonic resonance which contributes to a significant amplification of voltage and current harmonics [5]. The amplified harmonic current and voltage may damage the power capacitor. Moreover, it may disturb the operation of neighboring equipments. Hence, the consideration of power capacitor installation should include harmonic analysis at the design stage [6]-[14].

In general, a common solution to avoid harmonic resonance is to add a reactor in series with the existing capacitor. This combination forms a tuned filter with a tuned frequency slightly below the most dominant harmonic frequency. However, the system parameters are dynamically changed as the power system configuration varies and loads are changed. Therefore the **harmonic resonance** might still occur even if the tuning reactor has been added to the capacitor [15].

Several methods have been introduced in the literature for harmonic resonance damping. A hybrid filter topology is presented in [16], which damps resonance and compensates harmonic current simultaneously. This filter topology needs a transformer in series with the capacitor to create a single harmonic trap. In [15], the implementation and control of an anti-resonance hybrid shunt capacitor system is introduced, in which a small-rating three-phase system is connected in series with Y connected shunt capacitors without any matching transformer. In [5], a new anti-resonance hybrid delta-connected capacitor bank is proposed for power factor correction (PFC) in low-voltage industrial systems.

Similar results (a better result) can be achieved by simpler controllers, as described in the present paper. Simple proportional controllers, without any limiter, together with small-rating anti-resonance inverters, in series with the delta-connected capacitor banks eliminate parallel and series resonances simultaneously. The effectiveness of the proposed controller, in reactive power compensation as well as harmonic resonance elimination, is validated by Simulation results.

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II. ANALYTICAL DISCUSSION

A. Description of the problem

Figure 1 shows the single phase equivalent circuit of the system for each harmonic. In this circuit i_h is the load harmonic current, v_h is the source harmonic voltage, L and C are source inductance and power factor correction capacitor respectively. Capacitor current is calculated by considering the effects of the load harmonic current and the source harmonic voltage separately. To obtain capacitor current (i_{hc}^{i}) caused by i_h, source voltage is shorted, resulting in Eq. (1).

$$i_{hc}^{i} = \frac{X_L}{X_L + X_C} i_h \tag{1}$$

Parallel resonance will occur when the denominator of Eq.(1) approaches zero. At this condition, amplitude of the harmonic current, circulating between the source and capacitor, may be several times the amplitude of the load harmonic current.

In order to obtain the effect of the source harmonic voltage on capacitor current, the harmonic current source (the load) is taken as an open circuit. Then, the harmonic current injected into the capacitor (i_{hc}^{v}) due to the source harmonic voltage can be derived as:

$$i_{hc}^{v} = \frac{1}{X_L + X_C} v_h \tag{2}$$

Series resonance will occur when the denominator of Eq.(2) approaches zero.

Resonance frequency in both parallel and series resonance can be derived as:

$$\omega_{resonance} = \frac{1}{\sqrt{LC}} \tag{3}$$

B. Elimination of Resonance

One of the solutions for damping resonance between the source inductance and capacitor is to use a resistor within the capacitor branch. This causes the high harmonic current to be suppressed. However, the conventional passive resistor will result in power dissipation not only at the harmonic frequencies but also at the fundamental frequency, degrading power efficiency.

The basic concept here is that the damping resistor is required to respond at the harmonic frequency only. To realize this concept, an inverter can be used in series with the capacitor, as depicted in Fig.2, and controlled in such a way that acts as a virtual resistance at harmonic frequency and short circuit for the fundamental current component.

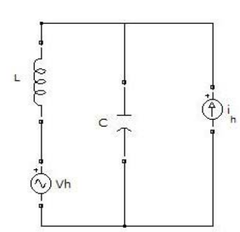

Fig. 1: single phase equivalent circuit of the system

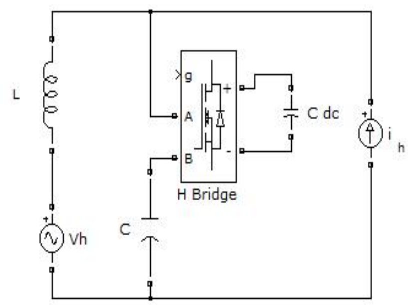

Fig. 2: H bridge inverter in series with capacitor for damping resonance

III. HYBRID CAPACITOR BANK

A. Power System Configuration

Figure 3 represents a common low voltage industrial system, comprising the 380V source with its impedance, a combination of linear and nonlinear loads and power factor correction capacitor banks. The load comprises 3 KVA linear with a lagging power factor of 0.8 and 500 W nonlinear, containing fundamental and 7th harmonic. A capacitor bank of 1.2 KVAR improves power factor up to 0.97 lagging. The utility voltage is distorted by 3% of 7^{th} harmonic. Some other system parameters are specified in Table 1.

B. Anti- resonance capacitor circuit

Figure 4 shows the system with anti-resonance devices. As discussed earlier, the series inverter suppresses capacitor resonance current by applying an opposite voltage into the circuit at the resonance frequency. At the fundamental frequency, the inverter must provide a short circuit for the capacitor. To achieve this, a pair of the adjacent switches at the top or bottom of the bridge must be kept on. According to these goals, proper switching signals are provided for the inverter.

Based on the parameters' values presented in Table 1, resonance frequency will be as follows:

$$f_{resonance} = \frac{1}{2\pi\sqrt{LC}} = 349.8 \text{ Hz}$$

This is very close to the 7^{th} harmonic and will cause a sever resonance due to the presence of the 7^{th} harmonics in the load current a source voltage.

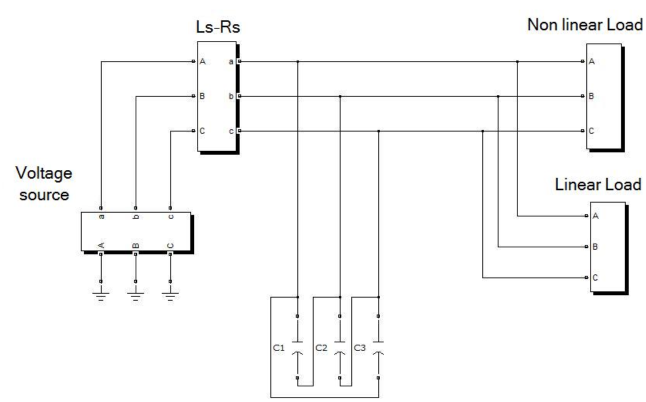

Fig.3: common low voltage industrial system

TABLE I. PARAMETERS SPECIFICATION

Source Impedance	
Source Inductance	***7.5 mH***
Source Resistance	***.15 Ω***
Capacitor bank	
Capacitor rating	***1.2 kVAR***
Capacitor C	***9.2 µF***
Connection type	***Delta***
Inverter	
Inverter rating	***150 VA***
DC capacitor	***4700 µF***
DC bus voltage	***50 V***
Switching frequency	***8.5 kHz***
Switching – ripple filter	
Filter capacitor	***1 µF***
Filter inductance	***1 mH***
Note: 3Φ, 380 V, 50 Hz	

C. Control strategy

Block diagram of the control system is presented in Figure 5. Three-phase capacitor currents are detected and transformed into dq0 reference currents i_C^d , i_C^q and i_C^o as follows:

$$\begin{bmatrix} i_C^d \\ i_C^q \\ i_C^o \end{bmatrix} = T \begin{bmatrix} i_{ac} \\ i_{bc} \\ i_{cc} \end{bmatrix} \quad (4)$$

$$T = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (5)$$

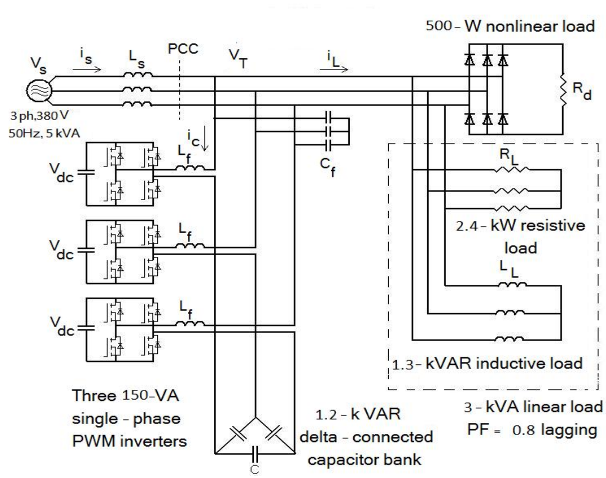

Fig.4: System schematic with anti-resonance power factor correction

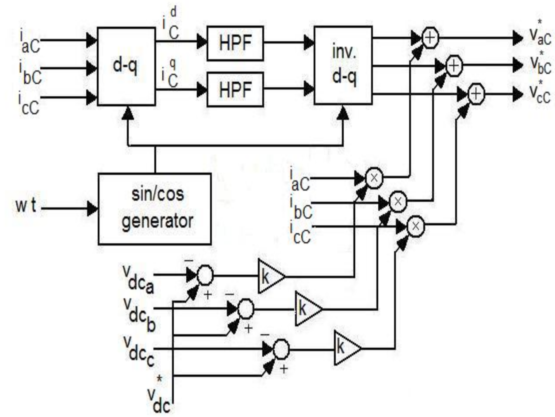

Fig.5: Control block diagram

Where ω is the line angular frequency. Two first-order high-pass filters with pass band edge frequency of 100 rad/s extract the harmonic component from i_C^d and i_C^q. After that, harmonic components are transformed into three-phase voltage references v_{aC}^* , v_{bC}^* and v_{cC}^* . In this section of control algorithm, to produce sufficient resistance to block harmonic current, unit gain is used. For compensating the inverter active power loss, therefore, keeping the inverter dc link capacitor voltage at the desired value, some active current at the fundamental frequency must be also absorbed from the source. To take this current into account, dc link capacitor voltage is compared with the desired value and the difference is added to the main current reference after passing through a proportional regulator and being multiplied by the corresponding line current.

IV. SIMULATION RESULTS

The system is simulated before and after employing the series inverters with the capacitor banks. With the power factor compensation capacitor alone, capacitor current contains a large amount of 7^{th} harmonic, as is shown in Fig.6. Specially, the current peak is unacceptably high and seriously dangerous for the capacitor itself. Employing a harmonic suppressing inverter in series with the capacitor, with the proposed control scheme, results in considerable reduction in the current harmonics, as indicated in Fig.7.

Simulation results are also summarized in Table 2 for comparison, including PCC voltage, capacitor current and source current, before and after employing the harmonic suppressing inverter. These results imply that the proposed control scheme successfully damps parallel and series resonance between the source reactance and power factor correction capacitance and reduces harmonics in the source current and voltage as well as the capacitor current to an acceptable level.

Inverter's dc link capacitor voltage together with the P.F. correction capacitor current, at start up, are shown in Fig.8. Harmonic suppression has been applied after about 7 cycles, during which the dc link capacitor has been charged up to the desired voltage.

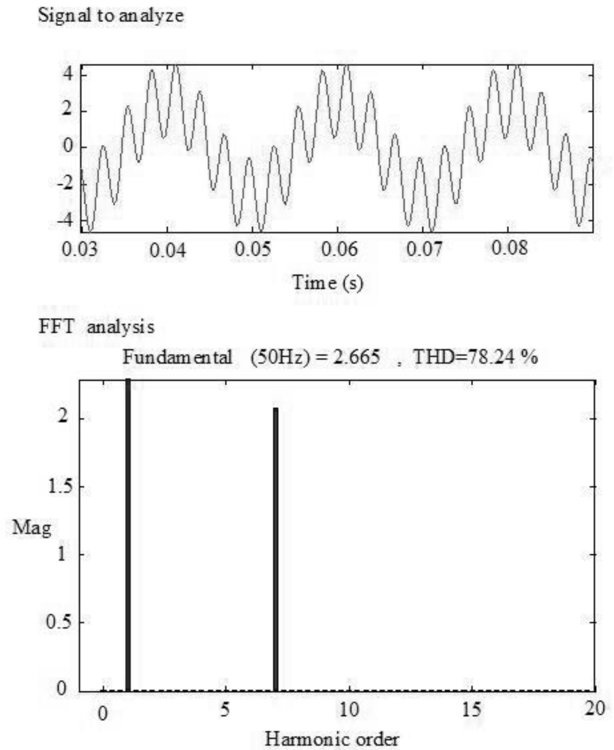

Fig.6: Capacitor current waveform and spectrum before employing harmonic suppressing inverter

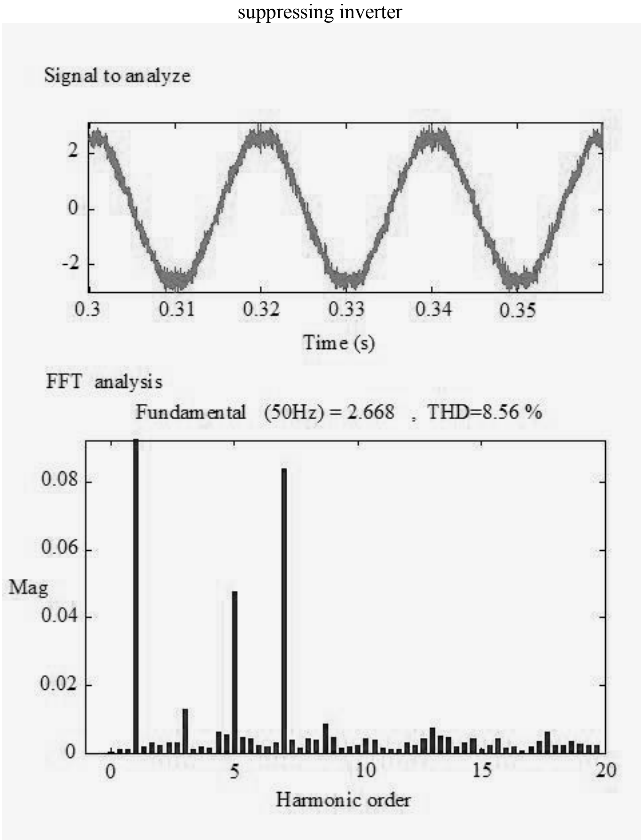

Fig.7: Capacitor current waveform and spectrum after employing harmonic suppressing inverter

TABLE II. SUMMARY OF THE SIMULATION RESULTS

Voltage and currents	P.F. correction capacitor alone			P.F. correction capacitor with harmonic suppressing inverter		
	1st	***7th***	***THD***	***1st***	***7th***	***THD***
$V_{pcc}[V]$	306.53	29.65	9.67%	306.53	7.24	2.67%
$I_c[A]$	2.67	2.09	78.24%	2.66	0.08	8.56%
$I_s[A]$	5.66	2.25	39.67%	5.69	0.31	5.52%

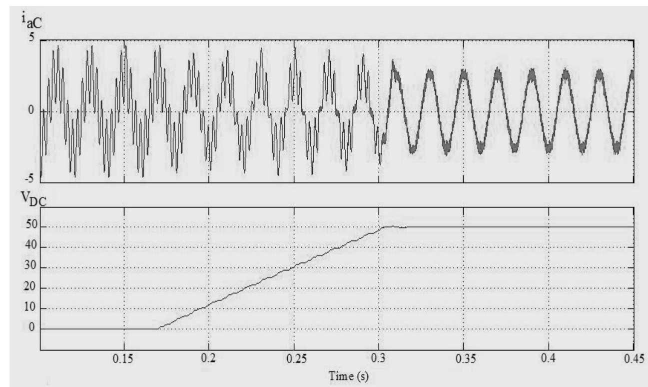

Fig.8: Inverter's dc link capacitor voltage and the main compensating current at start up

Transient response of the system is depicted in Figure 9. A sudden load increase of 50% has been applied at t=0.305s and returned back to the previous value at t=0.4s. As it is seen, it has a minor effect on the system operation.

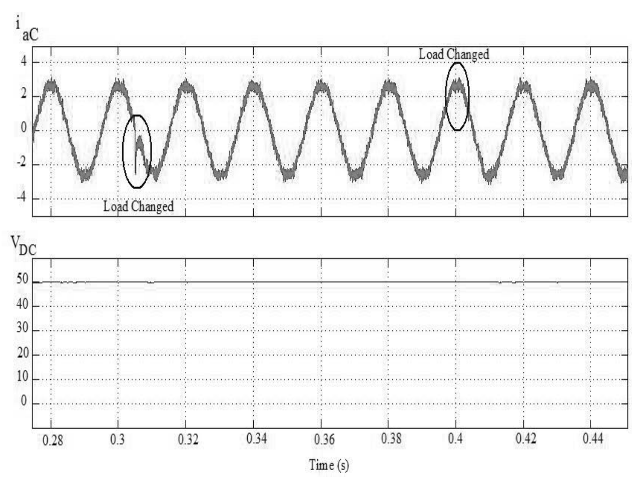

Fig.9: Response of the system to load changes at 0.305s and 0.4s

V. CONCLUSION

In this paper a simple control scheme has been proposed for an anti-resonance hybrid power factor compensator in low voltage industrial power systems. Parallel and series resonance between the P.F. correction capacitor and the source inductance, exited by nonlinear loads current harmonics as well as the source voltage harmonics have been examined. The proposed scheme is capable of successfully suppressing harmonic currents, while the capacitor does it normal task, i.e. reactive power compensation. The system performance has been evaluated by computer simulation. The results indicate a good performance both at steady state and transient.

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