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A New SPICE Macro-model for the Simulation of Single Electron Circuits

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To get a more accurate model for the simulation of single electron transistors (SETs), we propose a new macro-model that includes an electron tunneling time calculation. In our proposed model, we have modified the previous models and have applied some basic corrections to the formulas. In addition, we have added a switched capacitor circuit, as a quantizer, to calculate the electron tunneling time. We used HSPICE for a high-speed simulation and observed that the simulation results obtained from our model match more closely with that of SIMON 2.0. We also could evaluate the time of electron tunneling through the barrier by using the quantizer. Clearly, our macro-model gives more accurate results than other models when compared with SIMON 2.0 and can be used for calculating the delay time of complicated circuits.

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I. INTRODUCTION

Single-electron tunneling devices exploit effects that arise due to the quantized nature of charge. Thus, single-electron technology deals with the control of the transport and the position of a single electron or a small number of electrons. The fundamental physical principles of single electronics are the tunneling effect and the Coulomb blockade, which have been observed and studied by Gorter *et al.* [1-3].

Single electron transistors (SETs) hold great promise for future nano-electronic circuits due to their small size, low power consumption, and ability to perform fast and sensitive charge measurements [4,5]. Increasingly, they are being used and proposed as measurement devices for quantum systems, including quantum computers and quantum dots, and cellular automata, and as logic elements in their own right as replacements for metal-oxide- semiconductor field-effect transistors (MOSFETs) [1,6,7]. The rapid advances in nano-scale fabrication technology expedite the realization of single-electron integrated circuits, and there are increasing demands for a compact and accurate SET model for the analysis and design for single-electron integrated circuits.

Fabrication of single-electron circuits is an expensive and time-consuming process, and because of that, computer-aided design and simulation tools have been developed in order to study these circuits [2]. Obviously, accurate and flexible SET simulation tools are needed to be able to quickly modify and/or update a SET model, design and verify new ideas, and test and characterize (larger) SET circuits [8].

Several compact models have been reported for the development of single-electron circuit simulators. Many models based on tunneling and quantum mechanics, such as SENECA by Fonseca *et al.*, MOSES by Chen *et al.*, and SIMON by Wasshuber *et al.* have been developed for SETs in order to gain more insight into the SET's characteristics [7,9-13].

SIMON and MOSES are popular SET simulation tools based on the orthodox theory and use a Monte Carlo method for circuit simulations and evaluations of other simulators [7,14]. In these simulators, Monte Carlo methods are used for the probability calculation of all the Coulomb islands in a circuit, but a great amount of

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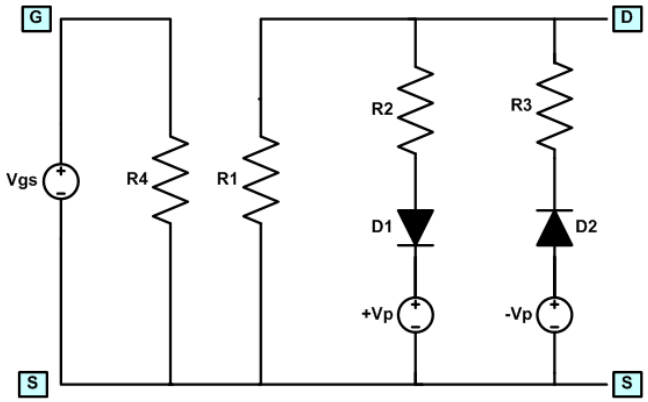

Fig. 1. Proposed macro-model of Yu *et al.* [15,16,18].

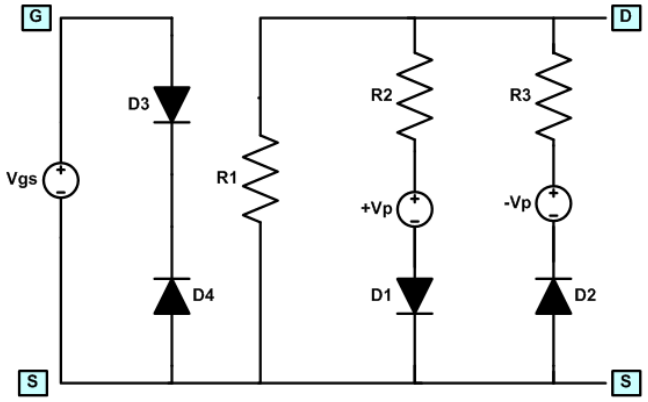

Fig. 2. Proposed macro-model of Wu and Lin [11].

simulation time is usually needed [3,9,10]. For efficient design and simulation of single-electron circuits, however, a compact and accurate model is required such as in the case of the conventional circuit simulators SPICE (simulation program with integrated circuit emphasis) [15,16].

In this manner, Macro-models and analytical SET models have recently been proposed and have been successfully verified in terms of their usefulness and accuracy [17]. Nevertheless, these models have their own disadvantages. In particular, Yu proposed a compact SPICE macro-model for SETs according to a parameter-based modeling and line-fitting method. Fig. 1 shows the macro-model of Yu *et al.* In the model, the interconnection among SETs was assumed to be large enough that each SET could be treated independently, and the results obtained were in good agreement with those obtained from the simulator KOSEC (Korea Single Electron Circuit Simulator) [12,15,18].

However, there are large discrepancies between the results obtained from the model of Yu *et al.* and those obtained from the well-accepted Monte-Carlo SET simulator SIMON. In the model of Yu *et al.*, the drain-source current, I_{ds}, increases linearly with the drain-source voltage, V_{ds}, in the Coulomb blockade region. For practical SETs, the I_{ds} should change exponentially with V_{ds} in the Coulomb blockade region. In addition, in the model of Yu *et al.*, the base line of I_{ds} increases as the gate-source voltage, V_{gs}, increases in the Coulomb oscillation characteristic of SETs due to the leakage current between the gate and the source of SETs [11].

To avoid the above-mentioned disadvantages of Yu *et al.*'s model, Wu and Lin proposed a modified and more accurate SPICE macro-model of SETs through a comparison with the results obtained from the SETs simulator SIMON 2.0. In Wu and Lin's SET macro model, which is given in Fig. 2, two face-to-face ideal diodes, D_3 and D_4, rather than the large resistor, R_4, in the model of Yu *et al.* are used to block all the possible current flows from the gate to the source in the SET. Results of this model are more accurate than those of Yu *et al.*'s [11].

However, in the model of Wu and Lin and in other mentioned models, SET devices are described by the orthodox theory of single electronics that is used to analyze and design circuits. In this theory, the time needed for the tunnel event is assumed to be zero [1,19]. For efficient design and simulation of SET, a compact and comprehensive model would be required. Therefore, to get a more accurate model that includes the electron tunneling time, we have proposed a new macro-model.

In Section II a new macro-model is proposed. Then, in Section III, we use our model for a general SET, extract simulation results for the terminal characteristics, and compare the results with those of SIMON and other proposed macro-models.

II. OUR SET MACRO-MODEL

A single-electron transistor, as shown in Fig. 3, consists of two small tunnel junctions and an "island" between them, usually with a third gate electrode capacitively coupled to the island. When the island of the SET is metallic (usually Al), it contains billions of electrons. The current between the source and the drain contacts can be controlled through the gate contact, making it possible to use the transistor as an amplifier; a small change in the gate signal induces a large change in the source-drain current. The functioning of the SET is based on the Coulomb blockade theory, which is a direct consequence of the discreteness of the electron charge. When an electron is added to the metallic island, this will create a difference in charge between the island and its environment, meaning that the capacitor between the island and the environment will be charged with a charge e [2,6,20-23]. The energy required to increase the charge on the capacitor of the central island by one electron, which is $E_C = (e^2/2C) \gg k_B T$, can be quite significant [1,23-25]. To travel from the source to the drain, electrons must overcome this charging energy barrier.

The operation of a SET involves only a few electrons,

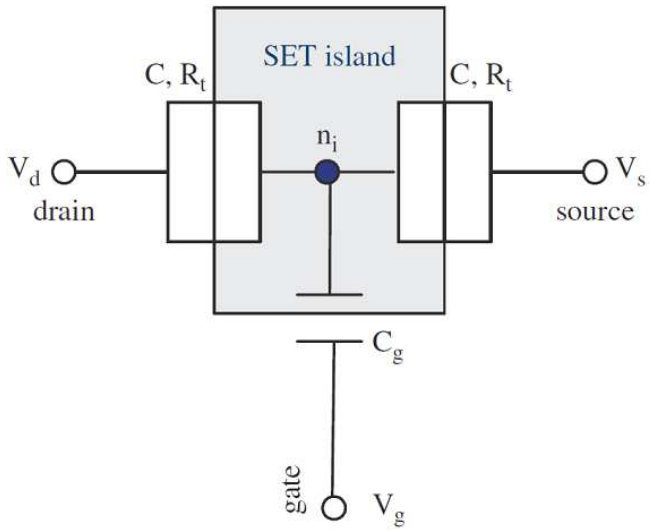

Fig. 3. Schematic of a SET.

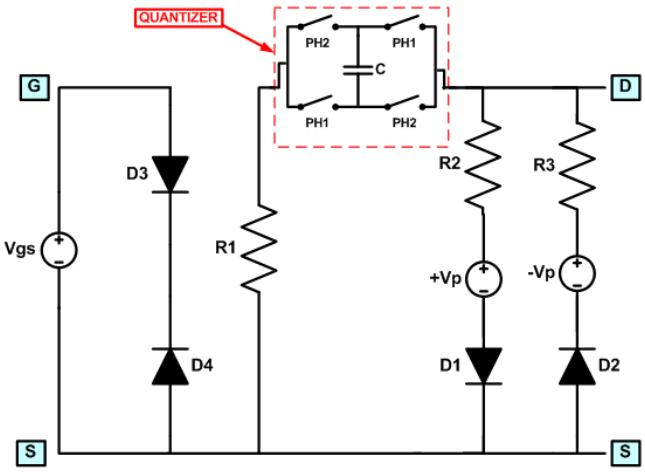

Fig. 4. Proposed SET SPICE Macro-model with quantizer block [26,27].

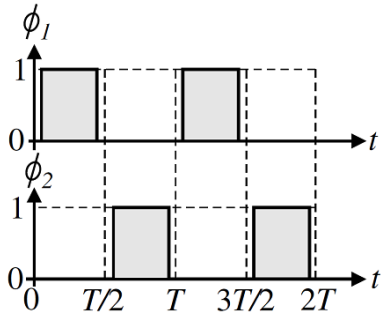

Fig. 5. Two-phase, non-overlapping clock scheme.

and its device characteristics are quite different from those of conventional metal-oxide-semiconductor (MOS) transistors, so in most of the literature on metallic SET junctions, the so-called 'orthodox' theory of single electronics is used to analyze and design circuits. In the orthodox theory, the time needed for the tunnel event is assumed to be zero. In a real situation, the main quantum property of the SET device is the phenomenon of electron tunneling and the time needed for the tunnel event is important, especially in complicated circuits, for delay time calculation. Our model explores the discrete character of the tunnel current and in contrast to the prescriptions, the tunneling time is not equal to zero in our model, and it can be evaluated.

The concept of our proposed model is based on the phenomenon that the circuit, including SET junctions, can be described by a discrete charge transfer through the tunnel junctions. During this discrete charge transfer, the tunnel event is modeled as a quantizer block to obtain a quantified output signal on the island. Therefore, in our proposed SET macro-model, which is given in Fig. 4, we have added a quantizer block to allow the tunneling-time calculation. This block consists of a bilinear-switched capacitor-resistor emulation circuit. In other words, the charge redistribution quantizer is a switched capacitor circuit, where the charge stored on a capacitor is used to perform the quantization. This macro-model has two face-to-face ideal diodes, D_3 and D_4, connected between the gate and the source to provide the advantages of Wu and Lin's model. Two branches consisting of combinations of resistors, diodes, and voltages are included between the drain and the source to provide symmetric features of the I_{ds}-V_{ds} characteristics [26,27].

R_1 and the equivalent resistance of the switched capacitor circuit are the primary resistors in the Coulomb blockade region. R_2 and R_3 are resistors of the SET in the non-Coulomb blockade region when its drain-source voltage V_{ds} is larger than a certain value, in the positive and the negative directions, respectively.

The bilinear-switched capacitor-resistor emulation circuit, quantizer block consists of four controlled switches and a capacitor, C. The switches are controlled by using the clock waveforms. There are two non-overlapping clock waveforms, Φ_1 and Φ_2, each one controlling two switches at the same time. The period of the clock waveforms is T, and the width of each individual clock is slightly less than $T/2$, as shown in Fig. 5.

The bilinear-switched capacitor circuit is equivalent to a resistor if the changes in the input and the output of the circuit can be neglected during the period T. On this condition, the equivalent resistance of the bilinear-switched capacitor-resistor circuit is $T/4C$.

It is noted that I_{ds} should be exponentially dependent on V_{ds} due to the tunneling of electrons through the tunneling junction [11]. To account for the exponential increase of I_{ds} as a function of V_{ds} inside the Coulomb blockade region, R_1, R_2, and R_3 have to be functions of V_{ds} as well. As shown in Fig. 4, R_1 is in series with the equivalent resistance of the bilinear-switched capacitor circuit, $CR_1 = T/4C$. To achieve the best compatibility, we have modified all resistors equations in our model as

follows:

$$\begin{aligned} R_1(V_g, V_{ds}) &= CR_2[\cos(CF.\pi.V_g) + Y] \\ &\quad \times 2^{(CV_P - Vds.x)}, \\ R_2(V_g, V_{ds}) &= R_3(V_g, V_{ds}) \\ &= \frac{CV_P}{CI_2 - 2CV_P/(R_1(V_g, V_{ds}) + CR_1)}. \end{aligned}$$

The switched capacitor equivalent resistance is given by $T_{sw}/4C$

$$\begin{aligned} &CR_1 = T_{sw}/4C, \\ &CR_2 = 1.33R_j(\text{For } \ T = 30 \text{ K}), \\ &CF \ = 2C_g/e, \\ &CV_p = 0.02 \end{aligned}$$

Here, Y is a positive parameter and a function of V_{ds}, X is a function of temperature, R_j is the junction tunneling resistance, C_g is the gate normal capacitance, T_{sw} is the period of the clock waveforms in the switched capacitor circuit. CR_1 and CR_2 are temperature-dependent parameters as specified in the model of Yu *et al.* [15]. The capacitance C in the switched capacitor circuit depends on the quantity CR_1 at the specified temperature.

III. SIMULATION RESULTS FOR THE TERMINAL CHARACTERISTICS

Figure 6 reveals the simulated I_{ds}-V_{gs} characteristics of SETs that were obtained by using our proposed model at $T = 30$ K. The Coulomb oscillation can be clearly seen from this figure. Fig. 7 compares the I_{ds}-V_{ds} characteristics obtained from SIMON 2.0, Wu and Lin's model, and our proposed model for both the Coulomb blockade and the non-Coulomb blockade regions.

The presence of the Coulomb blockade in the I_{ds}-V_{ds} characteristics of the SET is a region of zero current for a range of small drain-source voltage biases. We extracted that the maximum width of the Coulomb blockade region and found it to be equal to $2Ec/e$, which is equal to CV_p in the proposed equations. In fact, when the drain-source voltage V_{ds} is larger than $CV_p/2$, the non-Coulomb blockade region will appear. This boundary value of V_{ds} was not pointed out in previously-mentioned models.

Since the current flowing from the source to the drain in a SET depends on the tunneling probability through both the drain-tunneling junction and the source-tunneling junction, the drain-source current I_{ds} should be an exponential function of drain-source voltage V_{ds}. In order to clarify the exponential shape of the I_{ds}-V_{ds} characteristics of SETs in the Coulomb blockade region and to compare our model with that of Wu and Lin, we re-plotted the I_{ds}-V_{ds} characteristics in Fig. 8 for $R_j = 100$ MΩ, $C_j = 1.6$ aF, $C_g = 3.2$ aF, and $T = 30$ K. For SIMON 2.0, Wu and Lin's model, and our proposed model, the exponential increase in I_{ds} as a function of V_{ds} in the Coulomb blockade region is obvious. We observed that the simulation results obtained from our model matched more closely with those obtained from SIMON 2.0, in comparison with Wu and Lin's model, particularly within the Coulomb blockade region. The reason is the modification we exerted on all resistor equations in our model, as mentioned in the last section.

By comparison with the results obtained from SETs simulator SIMON2.0, our proposed model can describe the I_{ds}-V_{ds} characteristics of SETs correctly in both the

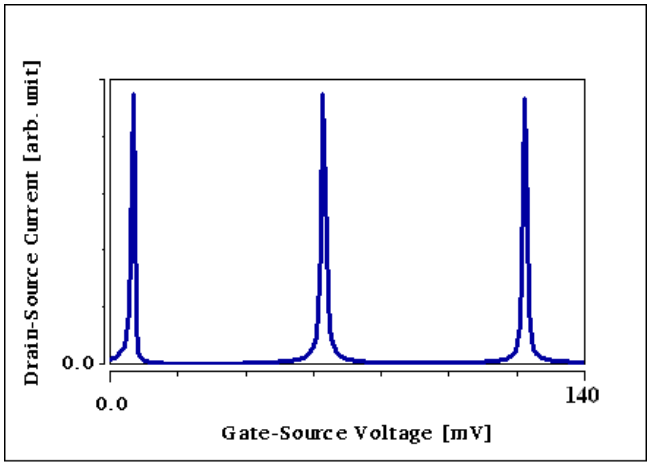

Fig. 6. Simulation result for the Coulomb oscillation of I_{ds} as a function of V_{gs}.

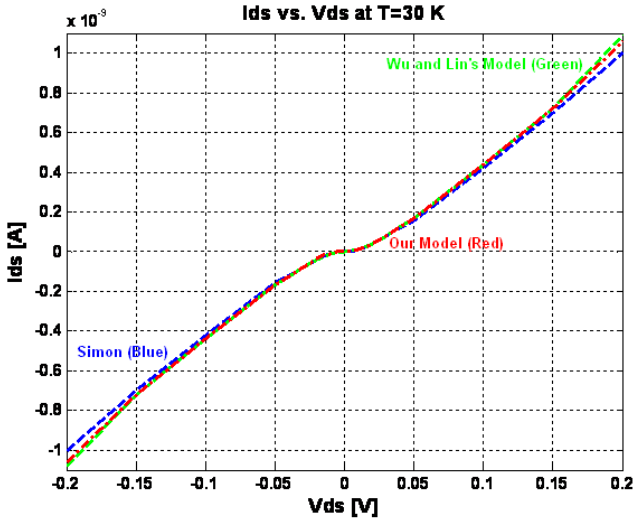

Fig. 7. Comparison of $I_{ds} - V_{ds}$ characteristics for both the Coulomb blockade and the non-Coulomb blockade regions, obtained from SIMON 2.0, Wu and Lin's model, and the proposed model under the conditions of $Rj = 100$ MΩ, $Cj = 1.6$ aF, and $T = 30$ K.

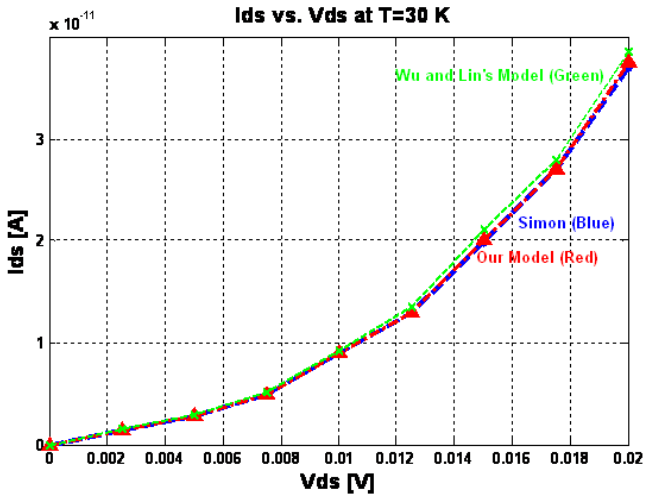

Fig. 8. Comparison of I_{ds}-V_{ds} characteristics in the Coulomb blockade region obtained from SIMON 2.0, Wu and Lin's model, and the proposed model under the conditions of $Rj = 100$ MΩ, $Cj = 1.6$ aF, and $T = 30$ K.

Coulomb blockade and the non-Coulomb blockade regions. Furthermore, the most important specification of our proposed model is the ability to perform a tunneling time calculation.

All events in the switched capacitor circuits are triggered by a clock signal. This means that although charge is transferred during one-half of the clock cycle, the result of this charge transfer will only be noticed at the rising (or falling) clock edge. For this reason, we decreased T, the period of the clock waveforms in the switched capacitor circuit step by step and checked the I_{ds} Coulomb oscillation. The minimum T such that the Coulomb oscillation can be observed is the real tunneling time. Certainly, the tunneling time depends on the temperature and the tunnel resistance. With our proposed model and the modified equations, it is possible to calculate the tunneling time at a specified temperature and tunnel resistance.

An additional advantage of our proposed model is the use of HSPICE as a simulator. We have chosen HSPICE software to develop a new SET macro-model because of its execution speed. HSPICE is a major advancement in modeling a complex system. The advantage is that the code will be compiled, so the simulation should be much faster than for other simulators such as MATLAB. Furthermore, it is a more stable and a more accurate tool. The use of a standardized language makes it possible to do a complete system simulation and makes the exchangeability of the code much easier.

IV. CONCLUSION

In this paper, we propose an improved SPICE macro-model for single electron transistors. A comparison with the well-accepted Monte-Carlo simulator SIMON 2.0 shows that our proposed macro-model can describe correctly the I_{ds}-V_{ds} and I_{ds}-V_{gs} characteristics of SETs, as well as the tunneling time. This model is especially suitable for calculating the delay time of complicated circuits.

Under the condition that the interconnections between single-electron transistors are large enough, our SPICE macro-modeling simulation provides an efficient way to analyze single-electron circuits, and the tunneling time evaluation can be achieved with reasonable accuracy. Therefore, those time-consuming calculations needed in Monte-Carlo simulation, can be avoided. Our model can also be easily modified for application to other SPICE software.

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