PSO/FDTD Optimization Technique for Designing UWB In-Phase Power Divider for Linear Array Antenna Application

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***Abstract*—This letter presents the design of a compact planar in-phase power divider with ultrawideband (UWB) performance. The device consists of three T-shaped microstrip lines arranged in parallel to each other on one side of the dielectric substrate that are electromagnetically coupled with an H-shaped slot etched on its ground plane. Particle swarm optimization (PSO) and the finite-difference time domain (FDTD) are combined to achieve the optimal power divider design for a given specification. The measured results show the transition of the signal between the T-shaped microstrip line and the ground-plane slot divides power equally, with relatively low insertion loss, good return loss, high stability of phase, and high isolation between the two output ports across the UWB frequency band defined between 3.1–10.6 GHz. The power divider is compact in size, occupying an area of 15×32 mm^2. These features make it suitable for linear array antennas.**

***Index Terms*—Microstrip, power divider, ultrawideband (UWB).**

I. Introduction

POWER dividers are extensively used in microwave circuits and subsystems such as antenna array feed network, mixers, amplifiers, phase shifters, and many other applications [1]. The most common power dividers are T-junction, hybrid ring, and Wilkinson [2], [3], which are classified according to the phase between their output ports as an in-phase or out-of-phase power divider. Due to the rapid growth of unlicensed use of ultrawideband (UWB) for short-distance wireless communications, there has been tremendous interest in exploration of various UWB components that operate in the UWB range, i.e., 3.1–10.6 GHz. For this purpose, wideband power dividers are needed.

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A popular power divider is the Wilkinson, which has good output matching and sufficiently high isolation, but its narrow bandwidth rules it out for UWB applications in its classical form. In recent years, extensive investigation has been done to develop and implement broadband Wilkinson power dividers. One method to broaden its bandwidth is to add open stubs [4]. A new three-way Wilkinson power divider that provides equal power slit over a wide bandwidth on a single-layer printed circuit board is presented in [5]. In [6], two dielectric substrates with a common ground plane have been used to achieve out-of-phase UWB performance. Recently, a Wilkinson power divider employing a pair of quarter-wavelength short-circuited stubs and/or parallel coupled lines to two symmetrical output ports was used to realize an UWB, i.e., 3.1–10.6 GHz, with good performance in terms of equal-power good isolation [7]. The structure, however, requires a resistor placed between two output ports.

A T-junction is a simple power divider, however it has poor isolation between its output ports [8]. Nevertheless, it has been combined with an electromagnetic coupling between a slotted ground plane and elliptical patch to realize an UWB planar in-phase power divider [9].

In this letter, a unique planar in-phase T-junction power divider is proposed. Unlike [7]–[9], the device uses no resistive elements and is compact in size. Finite-difference time domain (FDTD) method was used here to analyze the power divider, and particle swarm optimization (PSO) technique is used to optimize the power divider structure. The proposed device's performance is confirmed using simulation and measured results across a band of 3–11 GHz. The power divider exhibits equal power division between the output ports, with an average insertion loss of 4.56 dB over 3–11 GHz band with a phase imbalance of $< 3^\circ$. Its return loss at the input and output ports is better than 10 dB across the UWB range; also over this range, the average isolation between the output ports is 11 dB. The novel power divider exhibits comparable performance to [7] and [9] with the benefit of being physically more compact when fabricated on the same dielectric substrate. These properties make the power divider a good candidate for applications involving linear array antennas.

This letter is organized as follows. In Section II, the power divider structure design is described. In Section III, the FDTD/PSO method is used to optimize the power divider. Section IV presents the numerical and experimental results to validate the proposed power divider. The conclusion is given in Section V.

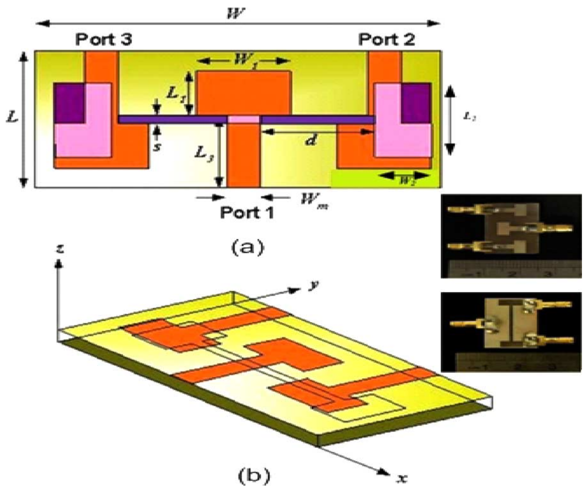

Fig. 1. Geometry of the proposed power divider: (a) top view and (b) 3D perspective.

II. Power Divider Structure

The geometry of the proposed power divider is shown in Fig. 1. Each one of the three ports of the power divider on the top layer of the substrate is connected to an open-circuit T-shaped microstrip line of length $L_1 \approx \lambda_g/4$ (λ_g is the guided wavelength at the center frequency of 6.85 GHz), which is placed at close proximity to each other with the center port inverted. The T-shaped structure consists of a microstrip line terminated with a capacitive square that provides effective electromagnetic coupling with the ground-plane slot. The bottom layer of the substrate constituting the ground plane includes one wavelength-long H-shaped slot line resonator that generates the first three resonant frequencies placed evenly within the desired UWB passband [15]. The H-shaped slot stretches under the T-shaped microstrip lines, where $W_2 \approx \lambda_s/4$ (λ_s is the guided wavelength of substrate at the center of frequency of 6.85 GHz). The purpose of the slot is to guide the coupled wave from the input port to the output ports. The shape of the slot determines its effectiveness to couple power over the UWB; this is achieved by terminating the slot line with rectangular slots with length quarter-wavelength, which provides the necessary transition between the slot and the top-layer microstrip.

The width (w_m) of the input and output microstrip ports corresponds to 50 Ω characteristic impedance. To achieve a good return loss at the microstrip ports, the slot of width (s) was chosen to have an impedance value close to 50 Ω, as seen from the microstrip line. According to [10], an appropriate transformation ratio n for microstrip-slot transition depends on the slot impedance and substrate characteristics. The transformation ratio is defined as

$$n = \sqrt{Z_{\rm ml}/Z_{\rm sl}} \tag{1}$$

where $Z_{\rm ml}$ is the microstrip impedance and $Z_{\rm sl}$ is the slot impedance.

For n of 0.7 and slot width of 1.1 mm, corresponding to an impedance 114 Ω, the impedance of the slot $Z_{\rm sl}$ as seen from the microstrip line is 55.86 Ω. The length and width of the open-end rectangular sections terminating the microstrip lines at the three ports are chosen to be a factor of the microstrip-line width w_m to enhance coupling with the ground-plane slot. In the initial design analysis, the dimension of W_1, W_2, L_1, and L_2 were chosen to be 6 mm ($2\times w_m$). The dimensions of the substrate are 34.5 × 15 mm^2. The power divider's performance is shown in Fig. 2. In its initial form, it is unsuitable for UWB application. Consequently, FDTD/PSO algorithm was used to optimize the power divider to achieve the desired performance and size reduction as described in the next section.

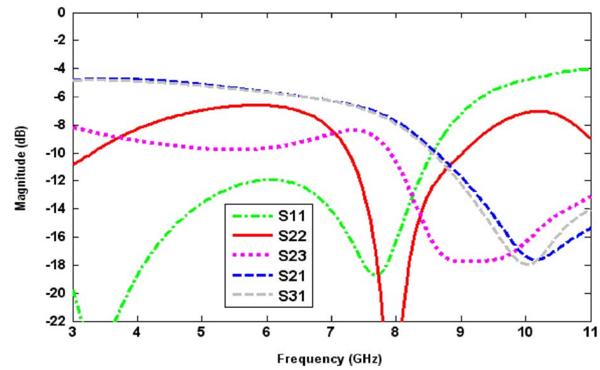

Fig. 2. Simulated performance of the initial power divider design.

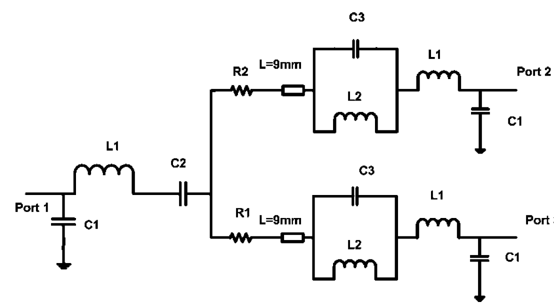

Fig. 3. Equivalent of circuit model of the proposed power divider.

To explore the response mechanism of the proposed power divider, its equivalent circuit was derived from simulation results using AWR's Microwave Office, as illustrated in Fig. 3. At port 1, the input microstrip line is modeled with series inductance $(L1)$ and shunt capacitance $(C1)$. As this microstrip line couples energy into the other two output port sections, it is represented with a series capacitance $(C2)$. Impedance matching is facilitated by resistance $R1$ and $R2$. The slot line is modeled with electrical length and characteristic impedance of Z_o and $\theta_{\rm sc}$, respectively. The parallel circuit represents electromagnetic resonance by the slot line. The optimized parameters of the circuit model are the following: $C1 = 0.07$ pF, $L1 = 0.6$ nH, $C2 = 0.93$ pF, $R = 46\,\Omega$, $L2 = 2$ nH, $C3 = 3.8$ pF, $Z_o = 114\,\Omega$, $\theta_{\rm sc} = 124.6°$.

III. FDTD/PSO Optimization

FDTD [11] was used to analyze and optimize the performance of the power divider. This electromagnetic modeling technique enables the specification of the material at all points within the computational domain and the effects of apertures to be determined directly and accurately. The FDTD code was developed for the proposed power divider structure, shown in Fig. 1, and includes convolutional perfect match layer (CPML) boundary conditions [12]. The CPML layers are eight cells thick on all six sides of the structure. The spatial step sizes Δx, Δy, and Δz are selected to be much less than the smallest

TABLE I
INITIAL AND OPTIMIZED VALUES OF DESIGN PARAMETERS

Parameters	W_1 (mm)	W_2 (mm)	L_1 (mm)	L_2 (mm)	D (mm)
Before-optimized	6	6	6	6	6
After-Optimized	8.1	4.35	3.75	6.99	8.45

guided wavelength λ_g. Spatial size steps were chosen to be $\Delta x = \Delta y = \Delta z = 0.4$ mm, and the time step was determined using

$$\Delta t = 0.95 \Big/ c\sqrt{(1/\Delta x)^2 + (1/\Delta y)^2 + (1/\Delta z)^2} \quad (2)$$

where c is the light speed in free space.

The FDTD code was written in FORTRAN 77 language to quickly perform the analysis. Four thousand steps of simulation were performed in about 2 min by running the code on a CPU E6550 2.33 GHz that had 4 GB of RAM. The PSO algorithm was written in MATLAB, which was linked with FORTRAN language to run the FDTD/PSO algorithm.

In the proposed power divider structure, the desired return loss of S_{11}, S_{22}, and S_{33} are less than 10 dB; bandwidth and flat insertion loss (S_{21} and S_{31}) covering the entire 3.1–10.6 GHz band are required. In order to achieve the required results, it was found that it is better to reduce the elements of fitness, as defined by

$$f_{\text{from } 3.1-10.6\,\text{GHz}} = 50 + \max(S_{11}) + \max(S_{21}) - \min(S_{21}). \quad (3)$$

The solution space is defined as: $W_1 \in (1,5) \times w_m$, $W_2 \in (1,5) \times w_m$, $L_1 \in (1,5) \times w_m$, $L_2 \in (1,5) \times w_m$, and $d \in (0.2, 0.8) \times \lambda_c$, where λ_c is the effective wavelength at the center frequency of operation. The dimensions of the substrate were fixed at $32 \times 15 \times 1.6$ mm^3. The algorithm was implemented with the utilization of "invisible boundary condition," where a particle is allowed to stay outside the solution space, the fitness evaluation of that position is skipped, and a bad fitness value is assigned to it [13], [14].

IV. EXPERIMENTAL RESULTS

A. Power Divider on FR4

The validity of the design methodology was tested by building the proposed power divider. The device was fabricated on FR4 with a thickness of 1.6 mm, dielectric constant of 4.4, and tangent loss of 0.02. As explained in Section III, FDTD/PSO was used to optimize the power divider. The optimized parameters are given in Table I.

The values of other parameters are $L_3 = 8.05$ mm and $s = 1.1$ mm. The fabricated power divider was tested and evaluated with its simulated performance.

The simulated and measured insertion loss of the power divider, shown respectively in Figs. 4 and 5, indicate that power is equally split between the two output ports across the 3–11 GHz band. The measured insertion loss between the input and output ports is ~5 dB across 3–11 GHz band. Also, the simulated and measured return loss of the input port and the two output ports are better than 10 dB across the whole UWB. The measured isolation between the output ports is 11 dB averaged over 3–11 GHz. The simulated and measured phase performance of the proposed power divider is shown in Fig. 6. There is less than $\pm 3^\circ$ phase difference between the output signals across the 3.1–10.6 GHz band. The novel power divider exhibits comparable performance to [8]. In addition, the area of the proposed power divider is reduced by about 20% in comparison to [8], which is 30×20 mm^2.

The loss of the proposed power divider was estimated by comparing the insertion loss of the device with PEC as the lossless material and with copper as the lossy material, which had

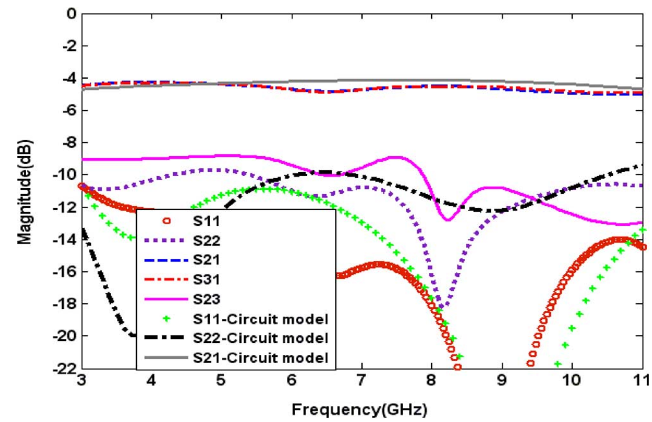

Fig. 4. Comparison between simulated and circuit modeled S-parameters of the proposed power divider.

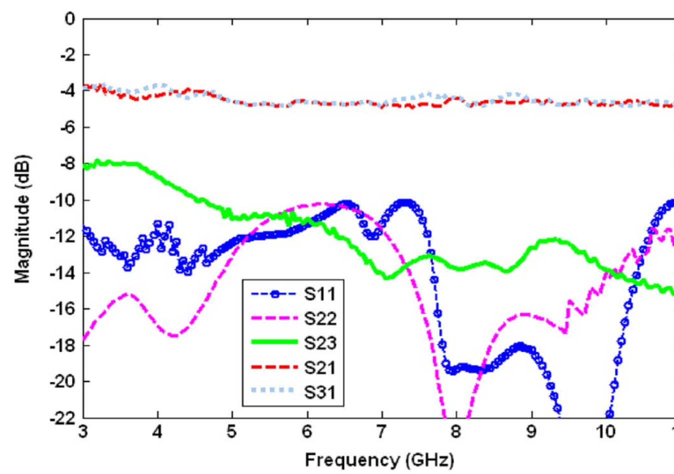

Fig. 5. Measured performance of the proposed power divider.

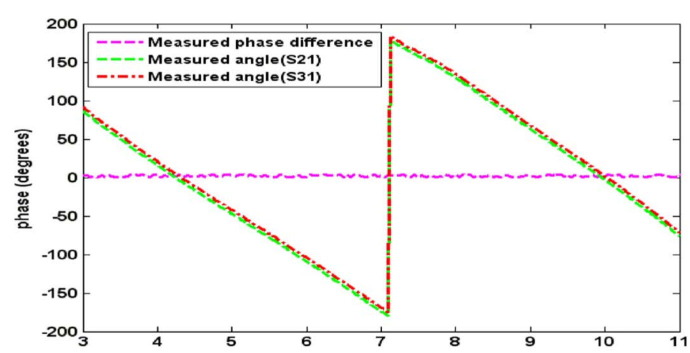

Fig. 6. Phase performance of proposed power divider.

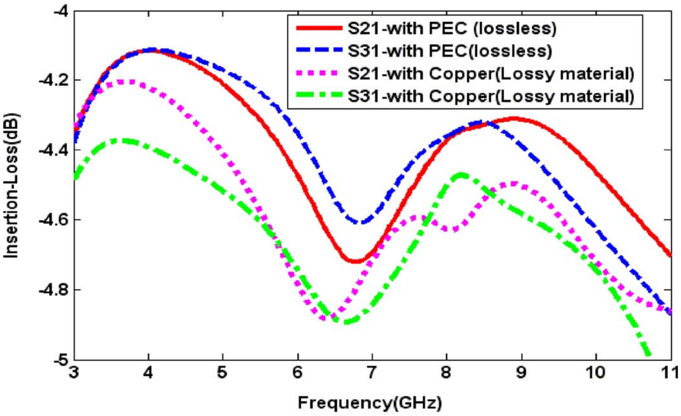

Fig. 7. Comparison of insertion loss using lossless material and lossy material.

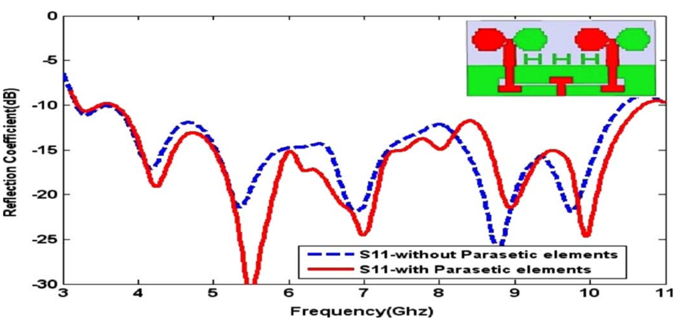

Fig. 8. Reflection coefficient of the UWB bow-tie antenna array using the power divider.

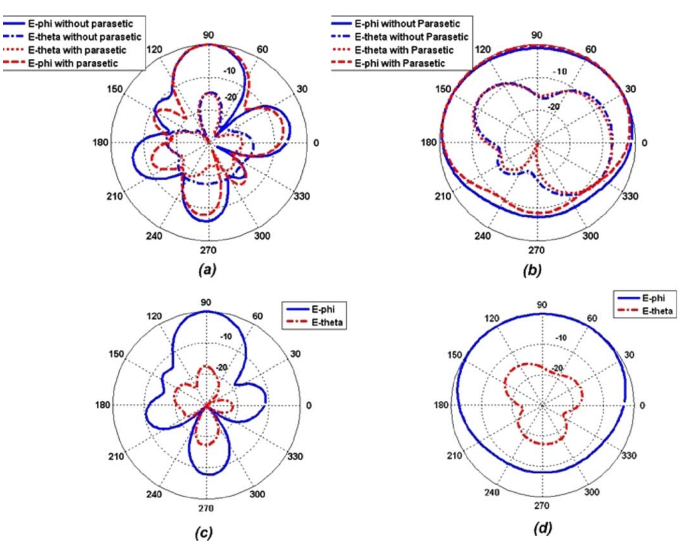

Fig. 9. Radiation pattern of proposed UWB bow-tie antenna array at 6 GHz with power divider and parasitic elements in (a) xy plane, (b) yz plane; and without power divider in (c) xy plane and (d) yz plane.

a thickness of 0.2 mm. The simulated results shown in Fig. 7 imply that with copper-based material, the loss increased marginally by 0.3 dB.

V. Application of Proposed Power Divider

The proposed power divider was utilized in an UWB bow-tie array antenna array 1×2 [13] fabricated on FR4 with dimensions of 66×43 mm^2, where the ground-plane dimensions are 66×17.5 mm^2. The configuration of the bow-tie antenna array is shown in Fig. 8. The center-to-center distance between the two antennas is 36 mm. The antenna configuration can be easily expanded to realize 1×4 and 1×8 arrays. The array's reflection coefficient, shown in Fig. 8, is below -10 dB. In the design, to suppress surface waves and decrease mutual coupling between arrays, we have used H-shape parasitic elements that are separated 10 mm from each other. The antenna's radiation pattern at 6 GHz with presence of the power divider with H-shape and without it and without the power divider in xy and yz planes is shown in Fig. 9. This implies that the gain of the antenna array will increase to a value of 0.75 dB at 6 GHz with use of H-shape parasitic element from 5 to 5.75 dB. This validates the application of the proposed power divider for UWB antenna arrays.

VI. Conclusion

Compact and UWB in-phase power dividers presented here comprisT-shaped microstrip lines electromagnetically coupled with the ground-plane H-shaped slot line. The device was optimized using FDTD/PSO method to meet certain design criteria. Across the 3–11 GHz band, the power divider exhibits equal power division between the output ports. On an FR4 board, the average insertion loss is less than 5 dB, and on RO4003 the average insertion loss is less than 4 dB. These devices exhibit return loss at the input and output ports better than 10 dB, and an average isolation between output ports of 11 dB. These characteristics make the device suitable for use in linear array antennas.

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