A 2.7 to 4.6 GHz Multi-Phase High Resolution and Wide Tuning Range Digitally-Controlled Oscillator in CMOS 65nm

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Abstract—**In this paper, a digitally-controlled oscillator (DCO) with differential output and eight different phases is proposed. The DCO is based on two-path ring oscillator (RO) with cross-coupled structure. The proposed DCO structure consists of four differential stages and two 9-bit digitally-controlled current sources, which guarantee high resolution and monotonic behavior of the DCO. The circuit is simulated in 65nm standard CMOS technology. The simulation results indicate that frequency can change from 2.7GHz to 4.6GHz with 512 steps which leads to very high resolution DCO. The simulated cycle to cycle Peak-to-Peak jitter and RMS jitter in 4GHz frequency are 6.47ps and 0.53ps respectively. Power consumption at 1.2v supply, varies between 0.59mW to 1.39mW based on digital code word.**

Keywords-multi-phase; differential; jitter; digitally-controlled oscillator; high-resolution; monotonic

I. INTRODUCTION

Many applications require oscillator with variable frequency as far as, controllable oscillators are the key block in digital processors to generate clock pulse and in communication systems to produce carrier signals. Due to the growing trend of digital circuits and many advantages of digital design for example, HDL implementation, improved testability, better reliability and noise immunity recently, there has been a thriving trend to design digitally controlled oscillator and all digital PLL (ADPLL) [1-3]. In ADPLL, DCO is the main block which determines ADPLL overall jitter, phase noise, tuning range, power consumption and area. Various topologies have been discussed to design DCO, Common structures in CMOS technology are LC based DCO [4] and ring based DCO [1]. Although LC based DCO shows low phase noise and high accuracy but lots of area which occupies by passive elements and limited frequency tuning range, and also the complex design process, has led ring based DCO to be more beneficial for many applications that don't require high accuracy. Ring based DCO has low power consumption and high integration capability and is the best option to produce multi-phase outputs with wide tuning range. Wide tuning range in RO based DCO will also improve reliability against PVT variation. Many applications such as, wireless communication systems [5] phase ADCs [6], and some digital processors need multiple high-frequency clocks. So, that was the motivation to design a high-frequency DCO with several different phases. Accordingly, we extracted a general model to map different ring oscillator phase and frequency association. Then we chose the best structure to fit specification that is described and by combining it with digital control techniques, we achieved a high resolution delay element for DCO. Accordingly, DCO's main weakness i.e., quantization noise reduced to a large extent.

This paper is structured as follows. The DCO design aspects will be reviewed in Section II. Section III describe the proposed DCO. Simulation results are presented in Section IV, and Finally, conclusions are presented in Section V.

II. DCO DESIGN ASPECTS

To discuss RO based DCO, two factors must be investigated:

A. RO structures

Ring based oscillator may be single-path (SPRO) or multi-path (MPRO) [7]. In SPRO to increase phases, number of stages should be increased. Although there is no restriction herein, but due to the inverse relationship between number of stages and maximum oscillation frequency then, by increasing stages, oscillation frequency will drop sharply. The solution in such case is MPRO. In MPRO structure for a fixed frequency, number of phases can be increased. or for a fixed number of phases, oscillation frequency can be increased Fig. 1 (e).

The simplest form of MPRO is the dual-path ring oscillator which divided into three general categories. First type is couple ring oscillator [8] Fig. 1 (a). In this structure, a number of rings are connected together by a second path. If increasing equivalent capacitor in nodes is ignored for simplicity, it can be said, in this structure oscillator frequency remains constant but number of phases have been increased. Second type is skewed delay oscillator [9] Fig. 1 (b), that will form by applying negative signal delay (in other words, a further phase, which is obtained from previous stages) to the oscillator nodes, so the oscillation frequency will increase for a constant number of phases. In this type of oscillators to achieve optimal performance, there needs to restructure inverter [10]. Third type is cross-coupled ring oscillator [11] Fig. 1 (c). The structure has tried to couple two rings by using cross-coupled inverters to achieve differential operation. Although number of phases has doubled but, due to the cross-couple latch effect, the frequency slightly reduced but the key feature is in the nature of symmetric and differential behavior of this structure, this

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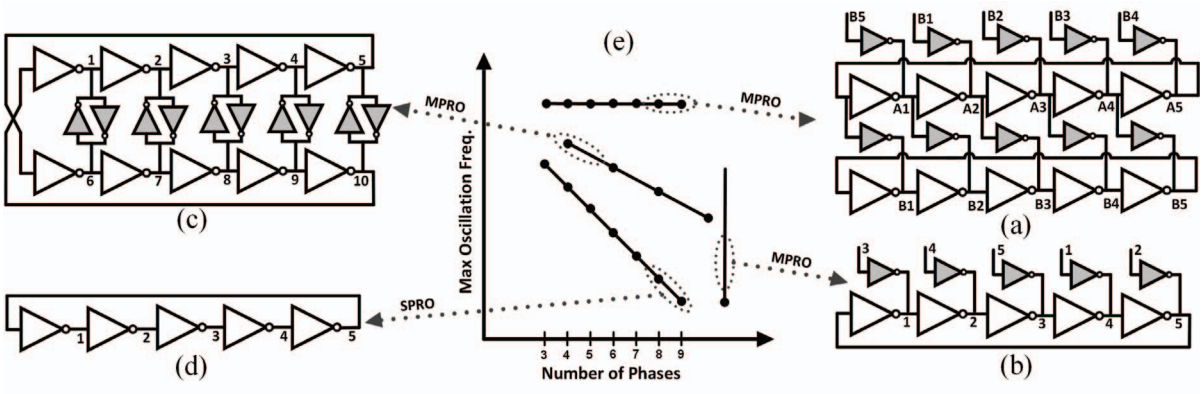

Figure 1. Dual-path ring oscillator a) Coupled oscillator. b) Skewed delay oscillator. c) Cross-coupled oscillator. d) Single path ring oscillator e) Conceptual relationship between number of phases and maximum oscillation frequency in SPRO and MPRO.

structure is the best choice for eliminating oscillator common mode supply and ground noises. Therefore, to reduce the biggest disadvantage of RO i.e., high phase noise and jitter, it can be helpful. All these three structures are based on a general model which was investigated in [7].

B. Digital control techniques for oscillators

As it is described, Control capability of the oscillator circuits can be done by digital code word which led to DCO design. In the following section, techniques for digitally changing oscillation frequency will be discussed. For simplicity, these techniques are based on SPRO. With regard to the oscillation frequency in SPRO equation (1), there are only two degrees of freedom to tune frequency of the oscillator. Number of stages (N) and each stages delay (t_d).

$$f_{osc} = \frac{1}{2Nt_d} \tag{1}$$

So, first technique is to change number of stages (N) in oscillation path [12] multiplexers or three-state buffers can be used to select the path with different number of elements Fig. 2 (a). Generally, this solution causes large frequency drift. Therefore, usually is used in combination with other methods. Second technique is to change stages' delay (t_d). Since t_d have direct dependency to nodes' capacitor and reverse dependency with charging current of nodes. Usually two methods to change t_d suggests: First method is using capacitor bank or hysteresis delay cell (HDC) bank Fig. 2 (b). Thus with the help of the digital code, equivalent nodes' capacitor changes and oscillator frequency is changed. Alternatively, by adding HDCs to the nodes, as a result of the latch effect of these cells, oscillator frequency is changed. Capacitor bank may be implemented with MIM capacitor [13] in this kind of implementation because the capacitor inherently doesn't produce noise thus, oscillator phase noise can be reduced. Capacitor bank can also implement by MOS capacitor [4, 14] but due to non-linearity of the MOS capacitor, oscillator accuracy is reduced. In full digital implementations with hardware description languages (HDL), capacitors usually Obtained by digital gates [1, 15]. In general, it's obvious that using of capacitor bank will occupy a lot of area on chip. To saving area [16] has used HDC to create a large delay steps and capacitor bank for fine tuning steps. Another alternative method to change t_d is using current sources Fig. 2 (c) [17]. Thus by changing digital code, current which charges and discharge nodes' capacitor changes and oscillator frequency is changed. The benefit is unlike capacitor bank which occupies a lot of area for wide tuning range, current source needs less area but the challenge is to design a monotonic behavior current source for all tuning range.

One of the weaknesses of digital oscillators than their analog counterparts, is quantization noise. The noise caused by dissociation in characteristic curve of the digital oscillator in the sense that the oscillator is only able to produce specific frequencies Fig. 3 (a), and doesn't have frequency continuity of analog oscillators Fig. 3 (b). So one of the challenges in DCO design is increasing number of control bits that increases the resolution characteristic curve and thereby reduce quantization noise. However, under normal circumstances increase control bits will cause non-linear characteristic curve so in most DCOs, a combination of described control techniques is used. but in this case nonlinear DCO characteristic is a new problem as far as, some DCOs forced to use linearization circuit [12].

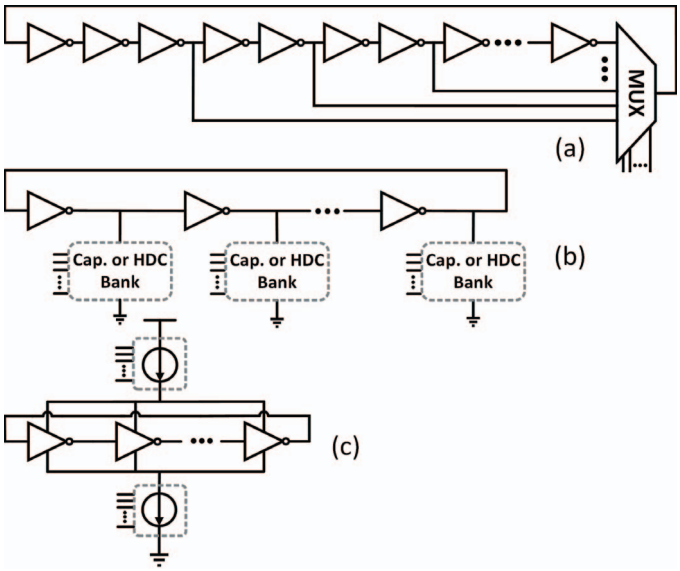

Figure 2. Digital control techniques to vary oscillator frequency. a) Path selection. b) Shunt capacitor bank or HDC bank c) Current starving.

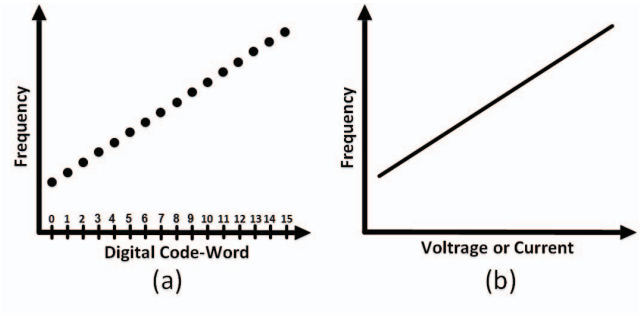

Figure 3. Ideal frequency characteristic of a) a digitally-controlled oscillator. b) an analog-controlled oscillator.

III. Proposed DCO Structure

In DCO design procedure, a few points should be considered:

- Low phase noise and low jitter performance.
- Wide tuning range.
- High resolution frequency variation.
- Reduced chip area.
- Reasonable power consumption.

With regard to the points mentioned in section II, to improve phase noise and jitter performance, we chose the cross-coupled structure as the DCO core, which form differential structure and so, improves the operation. And to achieve a wide tuning range with high resolution, we are going to use programmable current source to control DCO frequency. The downside of using a current source is static power consumption but due to high operating frequency of the DCO, static power is negligible compared with switching power consumption and contribution very small part in whole power consumed. According to the points discussed, conceptual block diagram Fig. 4, is suggested. The core element is two driver inverters and two cross-coupled inverters.

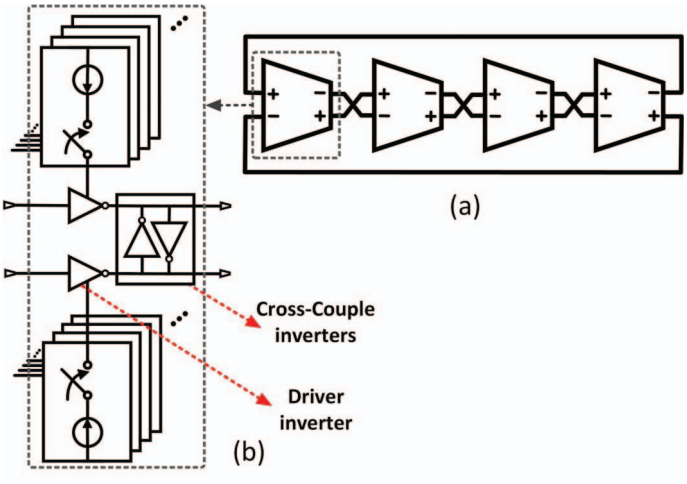

Figure 4. a) Conceptual four stages DCO. b) Gate level current-controlled differential delay cell.

The major delay in this element, resulting from the cross-coupled inverters which behave like a latch. Delay in latch like cross-coupled part, further investigated in Sense Amplifier Circuits [18] and derive from equation (2).

$$\tau = \frac{C}{g_m} \tag{2}$$

According to the equation (2) to reduce latch like element delay, capacitance of the nodes should decrease or g_m should increase. Thus, to control overall element delay, we chose current source to increase g_m indirectly by enlarging nodes current. Of course, in implementation, to achieve better efficiency, the current supply is applied to the driver inverters instead of adding directly to the nodes Fig. 4 (b).

According to the previous discussions, the final proposed DCO structure is composed of four differential cells and two high resolution 9-bit binary-weighted digitally-controlled current sources Fig. 5 (a).

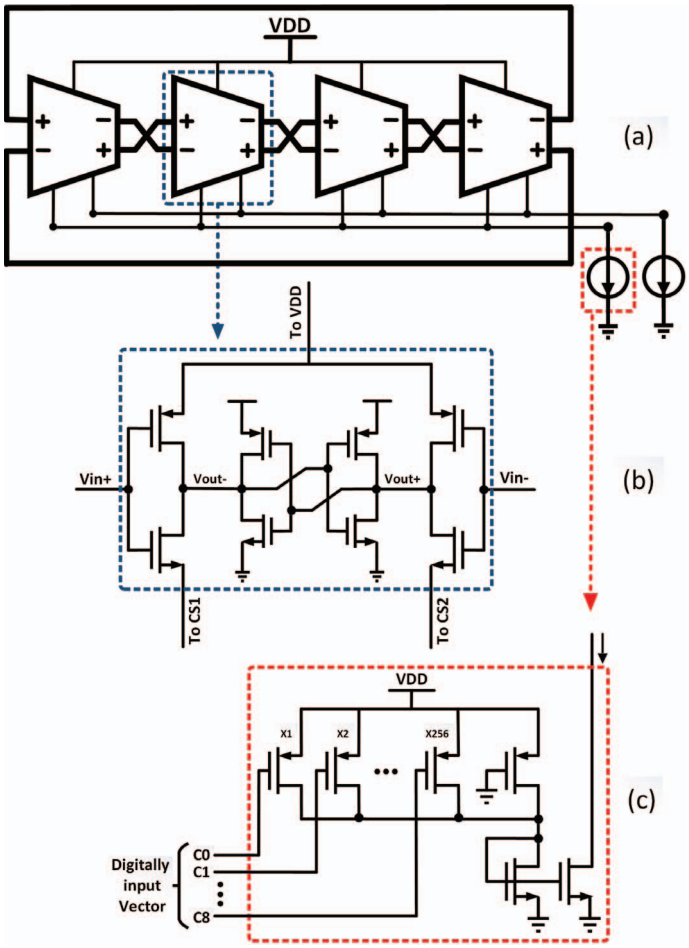

Figure 5. a) Proposed DCO with differential delay. b) Differential cell transistor level implementation. c) 9-Bit digitally-controlled current source transistor level implementation.

Each differential cell is composed of four inverters which transistor level circuit is shown in Fig. 5 (b). To reduce the area occupied by current sources each one can be shared among several inverters. Thus, only two digital current sources are needed for all four stages. Generally, digitally controlled current sources implement by paralleling binary-weighted transistor array Fig. 6. In such a current source, by changing digital code words, total current at the output node changes but the point is that the capacitance of the output node also will change. To solve this problem, we used current source structure introduced in [19], in our design Fig. 5 (c). In this current source the sensitive point only connected to one transistor that is always on, and the binary weight transistors have been isolated from the sensitive point so, output capacitor is fixed and doesn't change by digital code word. This structure helps to preserve DCO characteristics linear, as well as increase number of digital control bits. By using this current source, we increased the number of control bits to 9-bit which form 512 different modes for the DCO, so resolution further increased.

IV. Simulation and Evaluation of Proposed DCO

Fig. 7 shows DCO frequency and period variation versus digital code word. Given the fact that the proposed DCO has 512 different modes, both curves can be seen as a continuous line and have smooth and monotonic variation so, the quantization noise is greatly reduced. In frequency diagram average slope is 3.65MHz/Code and due to the concave curve, changes between minimum 1.5MHz/Code and maximum 7.7MHz/Code. Actually, this slope indicates DCO resolution and further reducing the slope means a higher resolution and fine frequency variation.

Fig. 8 shows DCO frequency variation versus digital code word for three process corners ss, tt and ff. in normal situation (tt) DCO output frequency can tune from 2.7GHz to 4.6GHz. Although in primary codes frequency has changed a lot for different corners, but thanks to the wide DCO tuning, overlap range between three corners still is acceptable range and eliminate this concern.

To evaluate DCO other parameters, the middle code word is used which, provides nearly 4GHz frequency at the output. Fig. 9, shows eye-diagram at 4GHz that is generated by overlapping output signal for one hundred thousand periods. The result indicates that the cycle-to-cycle Peak-to-Peak and RMS jitters are 6.47ps and 0.53ps respectively.

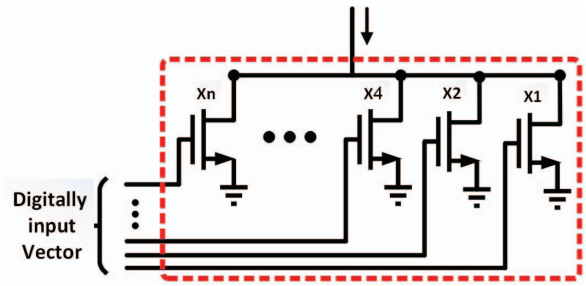

Figure 6. Conventional digitally-controlled current source.

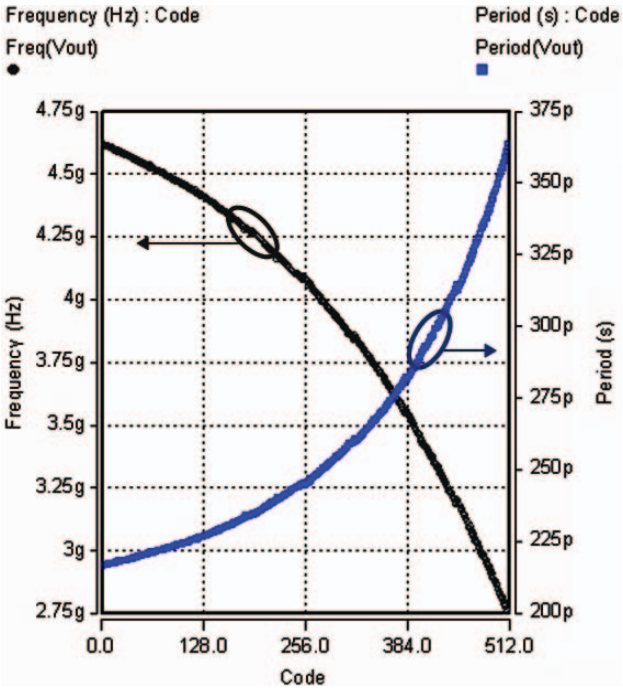

Figure 7. DCO characteristic chart.
frequency vs. code word and period vs. code word.

Monte Carlo simulation analysis for 1000 runs at 4GHz has been done with complete model that gives the whole circuit mismatch and variation, Fig. 10. The result indicates most runs are between 3.8GHz to 4.4GHz.

Fig. 11, shows power consumption versus digital code word. As was predictable, according to the case that main power consumption in digital circuits caused by switching activity, the maximum power consumption of the DCO occurs in high-frequencies that is 1.39mw and minimum power consumption occur in low frequencies and is equal to 0.59mw.

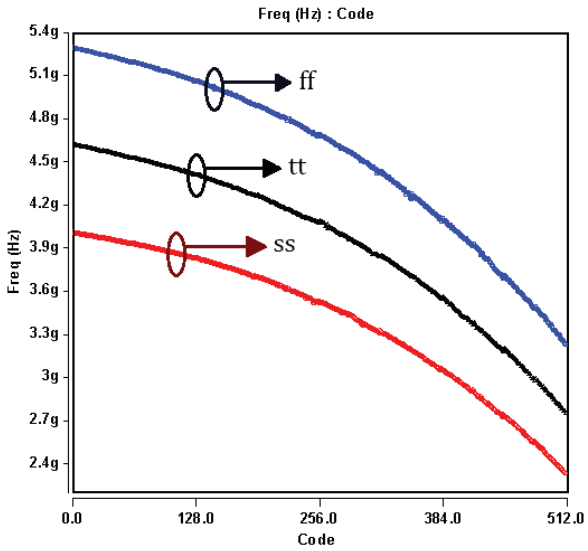

Figure 8. DCO characteristic chart for ss, tt and ff process corners.

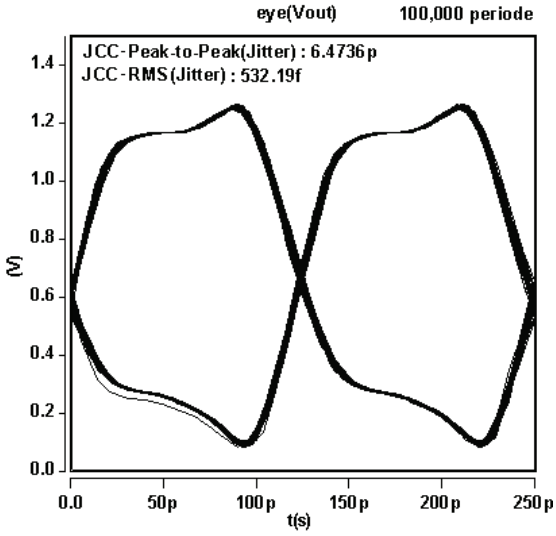

Figure 9. DCO eye-diagram at 4GHz frequency shows peak-to-peak jitter and RMS jitter are 6.47ps and 0.53ps respectively.

Finally, in Table I, the proposed DCO simulation results are compared with other recent references. Power consumption is less compared to the other, and of course maximum operation frequency is increased. Based on number of control bit and coding type and variation range, the proposed DCO shows low quantization noise means higher resolution in tuning.

V. CONCLUSION

In this work, a Digitally-Controlled Oscillator (DCO) is presented, which is composed of four differential cells and two high resolutions digitally controlled current sources helps to develop a DCO that has high resolution and can tune from 2.7GHz to 4.6GHz by 512 steps. Furthermore, DCO provides eight different phases at the output. Simulation results show

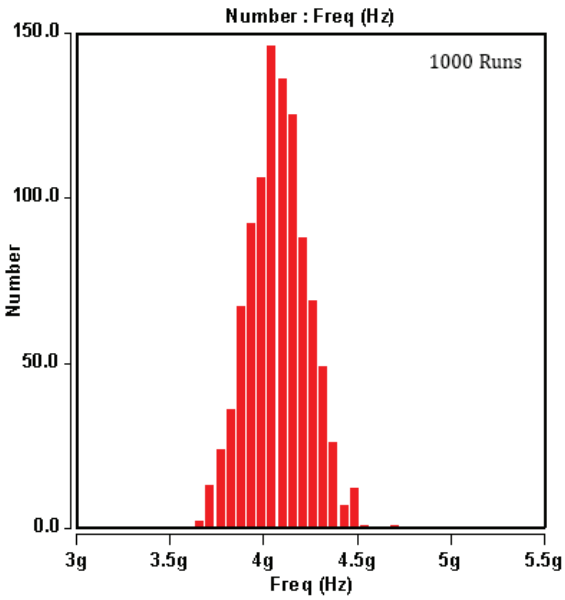

Figure 10. DCO Monte Carlo analysis at 4GHz frequency by 1000 runs with complete Monte Carlo model.

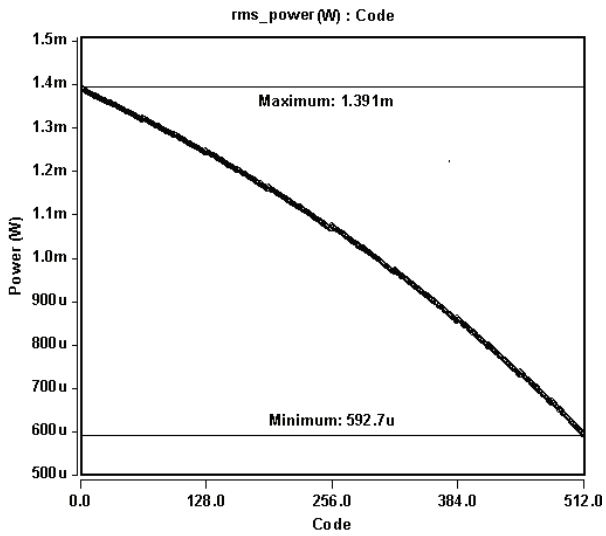

Figure 11. DCO RMS-Power vs. Code word. maximum and minimum power are 1.39mW and 0.59mW respectively.

that due to differential operation, jitter is improved to a great extent and cycle-to-cycle Peak-to-Peak and RMS jitters are 6.47ps and 0.53ps respectively. The target application could be digital systems which need ADPLL with low quantization noise and multiple outputs.

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TABLE I. PERFORMANCE COMPARE WITH EXISTING DCOs

Items \ Type	*Proposed*	*[14]' 2015*	*[3]' 2014*	*[20]' 2011*
Technology	**65nm**	65nm	65nm	90nm
Supply Voltage	**1.2v**	1.2v	1v-2.5v	1v
Results	**Simulation**	Experimental	Experimental	Simulation
DCO control bits	**9bit binary**	8bit binary	10bit binary	30bit(coarse) one-hot + 32bit (fine) binary
Frequency range	**2.7GHz ~ 4.6GHz**	1.5GHz ~ 3.5GHz	2.2GHz ~ 3GHz	0.22GHz ~ 1.52GHz
Oscillator Phases	**8**	8	8	1
Jitter & Power Measure @	**4GHz**	2.5GHz	2.24GHz	1.52GHz
PK-to-PK Jitter	**6.47ps**	29ps	77.5ps (ADPLL)	N.A.
RMS Jitter	**0.53ps**	2.8ps	8.9ps (ADPLL)	N.A.
Power	**1mW**	6mW	2.3mA*VDD	0.79mW

REFERENCES

[1] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, et al., "A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique," IEEE Journal of Solid-State Circuits, vol. 50, pp. 68-80, Jan. 2015.

[2] H. Yi-Chieh, L. Che-Fu, H. Hsien-Sheng, and W. Ping-Ying, "A 2.4GHz ADPLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, Feb. 2014, pp. 270-271.

[3] A. Kavala, W. Bae, S. Kim, G.-M. Hong, H. Chi, S. Kim, et al., "A PVT-compensated 2.2 to 3.0 GHz digitally controlled oscillator for all-digital PLL," Journal of Semiconductor Technology and Science, vol. 14, pp. 484–494, Aug. 2014.

[4] J. H. Han and S. H. Cho, "Digitally controlled oscillator with high frequency resolution using novel varactor bank," Electronics Letters, vol. 44, pp. 1450-1452, Dec. 2008.

[5] L. Wei-Chang, Y. Fu-Chun, W. Ting-Chen, H. Ya-Shiue, L. Tai-Yang, H. Shen-Jui, et al., "A SC/HSI dual-mode baseband receiver with frequency-domain equalizer for IEEE 802.15.3c," in Circuits and Systems (ISCAS), 2013 IEEE International Symposium on, Beijing, May 2013, pp. 793-796.

[6] B. Banerjee, C. C. Enz, and E. Le Roux, "Detailed analysis of a phase ADC," in Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on, Paris, May 2010, pp. 4273-4276.

[7] A. A. Hafez and C.-K. K. Yang, "Design and Optimization of Multipath Ring Oscillators," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, pp. 2332-2345, Oct. 2011.

[8] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," IEEE Journal of Solid-State Circuits, vol. 28, pp. 1273-1282, Dec. 1993.

[9] L. Seog-Jun, K. Beomsup, and L. Kwyro, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," IEEE Journal of Solid-State Circuits, vol. 32, pp. 289-291, Feb. 1997.

[10] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," IEEE Journal of Solid-State Circuits, vol. 44, pp. 1089-1098, Apr. 2009.

[11] D. Liang and R. Harjani, "A low-phase-noise CMOS ring oscillator with differential control and quadrature outputs," in ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International, Arlington, 2001, pp. 134-138.

[12] M. Souri and M. B. Ghaznavi-Ghoushchi, "A 14.8 ps jitter low-power dual band all digital PLL with reconfigurable DCO and time-interlined multiplexers," Analog Integrated Circuits and Signal Processing, vol. 82, pp. 381-392, Feb. 2015.

[13] M. E. S. Elrabaa, "A portable high-frequency digitally controlled oscillator (DCO)," Integration, the VLSI Journal, vol. 47, pp. 339-346, June 2014.

[14] M.-C. Su, S.-J. Jou, and W.-Z. Chen, "A Low-Jitter Cell-Based Digitally Controlled Oscillator With Differential Multiphase Outputs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, pp. 766-770, Apr. 2015.

[15] C. Pao-Lung, C. Ching-Che, and L. Chen-Yi, "A portable digitally controlled oscillator using novel varactors," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 52, pp. 233-237, May 2005.

[16] S. Duo, C. Ching-Che, and L. Chen-Yi, "An Ultra-Low-Power and Portable Digitally Controlled Oscillator for SoC Applications," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, pp. 954-958, Nov. 2007.

[17] A. Tomar, R. K. Pokharel, O. Nizhnik, H. Kanaya, and K. Yoshida, "Design of 1.1 GHz Highly Linear Digitally-Controlled Ring Oscillator with Wide Tuning Range," in Radio-Frequency Integration Technology, 2007. RFIT 007. IEEE International Workshop on, Rasa Sentosa, Dec. 2007, pp. 82-85.

[18] A. Hajimiri and R. Heald, "Design issues in cross-coupled inverter sense amplifier," in Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on, Monterey, Jun 1998, pp. 149-152 vol.2.

[19] M. Maymandi-Nejad and M. Sachdev, "A monotonic digitally controlled delay element," IEEE Journal of Solid-State Circuits, vol. 40, pp. 2212-2219, Nov. 2005.

[20] S. Duo and L. Jhih-Ci, "A monotonic and low-power digitally controlled oscillator with portability for SoC applications," in Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on, Seoul, Aug. 2011, pp. 1-4.