A 35.6dB, 43.3% PAE Class E differential Power Amplifier in 2.4GHz with Cross Coupling Neutralization for IoT Applications

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Abstract—**In this paper a novel class E power amplifier with high efficiency and low power consumption for internet of things (IOT) application is presented. It is shown that employing cross coupling neutralization and fully differential topology in class E power amplifier lead to high power efficiency, high power gain and better reverse isolation. The proposed class E amplifier can achieve 28.5 dBm output power to a 50Ω load at 2.4 GHz with 43.6% power added efficiency and 35.6 dB power gain. These results are verified by the circuit level simulations of the proposed PA that performed by 0.18µm standard CMOS technology.**

Keywords-PA; Internet of things; Efficiency; neutralization; cross coupled;Fully differential;class E.

I. INTRODUCTION

IoT is one of the important practical issues in academic research that is consisted of several different components. Transceiver is a major component in IoT devices which contains a number of blocks, including LNA, ADC, mixer, Power amplifier and etc. A lot of research about the internet of things devices (IOTD) has been concentrated on IOT RF transceiver design. The power amplifier (PA) is one of the most critical building blocks of the transceiver. PA consume most power in the transceiver component. Therefore, the high efficiency PA could warrant a long working time of the portable device in IOTD. The amplifiers can be classified into two main groups: linear amplifier which consist of class A to C and switch type amplifier which comprised class D and E. Class F PA fall between linear and switch amplifier. The first group of amplifier consist of conventional class A.B, AB and C operation mode, which the transistor is working as current source [1]. The linearity of these PA's is good, but they have poor efficiency. On the other hand linearity of switching type PA is poor, but efficiency is high compare to first group PA. Firstly, Sokal in 1975 was introduced a class E power amplifier [2]. By attention to high frequency operation of class E PA and their simplicity structure, these classes of PA's are suitable choice for employing in high frequency transmitter [3-13]. Recently, high frequency and high efficiency power amplifier are proposed. Some techniques such as mode blocking has been introduced to achieve high frequency PA [14]. But, frequency bandwidth is limited is limited by locking range of mode lock-base power amplifier.

A lot of circuit structure and design technique have been presented for class E PA .In the conventional structure an RF choke is used between the supply voltage and switch transistor. This is recognized as an infinite DC feed or shunt capacitor architecture. These circuits is not proper for integration design because the available chokes don't have a high quality factor inductor. So, power consumption of this architecture is too high [15]. In the modified structure a small inductance inductor is used and eliminate choke without any shunt capacitance. This structure couldn't reach desirable result, because of capacitance of drain node [15]. Another structure takes the advantage of two former architectures. In this architecture a small shunt inductor and a shunt capacitor are employed in drain mode [16-18]. Parallel circuit [17] and even harmonic are two design techniques of these architectures which is called second order finite DC feed by some reference [19]. This paper presents a fully differential class E PA. The complimentary CMOS cross couple pair configuration is used to accomplish the LC tank oscillator to have lower THD [14]. By using this technique high operating frequency of PA is achievable while PAE and PA pout are high too. On the other hand a capacitor cross coupling neutralization is applied to enhance power gain and stability. As seen in pervious papers each design could better one of the character of PA but in this work by using combination of these techniques high gain, high PAE, high pout and low power consumption are provided concurrently. Only area of our design may be negative point because of capacitor using.

The rest of this paper is organized as follows. Section II describe a concise review of the class E power amplifier. This section is continued by a detail illustration of our proposed PA circuit. Simulation results are demonstrated in section III and concluding remark are derived in section IV.

II. CIRCUIT DESCRIPTION

A. Basic theory of class E power amplifier

A typical configuration of class E PA is shown in Fig. 1. The idea behind class E PAs is to soften the hard switching requirements imposed on the transistors or in other word class E PA utilize the harmonic content in order to sharp the voltage and current waveforms and this technique is lead to obtain high efficiency and decrease power consumption, consequently.

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Because of this a parallel LC tank tuned to the third harmonic is added to this structure to get third harmonic component and add them to the fundamental signal of PA. Several issues have to be realized for power amplifier to be classified as class E.

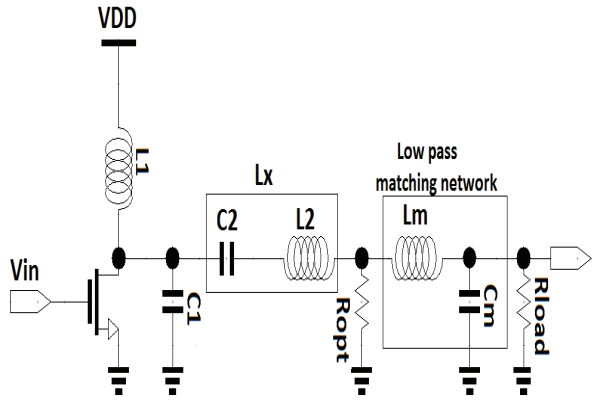


Fig. 1. A typical configuration of class E power amplifier

First, if transistor switch turn off, the voltage through the switch should remain low and when the switch turn on, voltage should be zero. Finally the first derived of drain voltage with respect to time is zero (dV_{ds}/dt), when switch is on and this equation conforms that voltage current product is minimized and by attention to mention point the switch dissipate no power ideally and the DC supply voltage is delivered to RF output. This concept is called "soft switching".

Class E PA achieves 100% efficiency theoretically in the expose of poor linearity performance. Transistor of class E PA has operated in triode region when switch is on. Therefore, power loss in this structure is inevitable.

L1 AND C1are tuned to resonate at the fundamental frequency while L_2 and C_2 are tuned to present non zero load impedance at third harmonic frequency to make up the second terms in the Fourier series expansion of the square wave.

$$L_x = \frac{\pi v_{dd}^2 (\pi^2 - 4)}{2\omega p_{out}} \tag{1}$$

$$C_1 = \frac{P_{out}}{\pi \omega v_{dd}^2} \tag{2}$$

$$R_{load} = \frac{0.577 v_{dd}^2}{p_{out}} \tag{3}$$

$$L_m = \frac{\sqrt{R_{opt}(R_L - R_{opt})}}{\omega} \tag{4}$$

$$C_m = \frac{\sqrt{\frac{(R_L - R_{opt})}{R_{opt}}}}{R_L \omega} \tag{5}$$

$$R_{opt} = \frac{8 v_{dd}^2}{p_{out}(\pi^2 + 4)} \tag{6}$$

Since many reference [5, 6, 11, 20] has completely analysis of class E power amplifier further analysis could be find in those research study.

Numerous advantages were introduced for differential topology. First of all, a common mode noise is minimized which reduce the disturbance of substrate coupling to another circuit. Because of twice current discharging in each cycle, interference to the desired signal is decreased. The breakdown voltage of the CMOS process is too low and by process scaling it would be even worse. But, the most advantage of differential structure is gain boosting, relaxes the stringent requirement on device breaking voltage. Another benefit of this configuration is double output power compared to single ended counterpart. In addition, the size of a transistor can be small because the current flow through the transistor is decreasing for the same supply voltage and the same output power. All of these reasons lead us to use differential structure for PA design.

By using cross coupling capacitor the effective trans-conductance of transistor increase and on the other hand power dissipation decrease, simultaneously [21]. In addition, it was shown that this structure utilizing lead to increase gain and improve reverse isolation [22]. The power amplifier transistors should have large size, so that the gate drain capacitance is extremely large, these capacitances are hundred femto Farad. These extra capacitance reduce the gain and deteriorate stability.

A lot of watt level power amplifier was reported with higher than 40% power added efficiency (PAE) which was used different CMOS technology such as 0.8um and 0.35um [23, 24]. In [23] robustness against voltage stress was obtained but power dissipation is large. Combining positive feedback with the class E PA configuration and injection lock oscillator is utilized to locked oscillation frequency with input signal [24]. This structure has more sensitivity to limit the voltage stress on the transistor. Therefore, delivering RF power for deep submicron CMOS power amplifier is still a challenge. Some references [24-26] use some millimeter wide transistor in order to drive sufficient current for watt-level output power.

III. PROPOSED FULLY DIFFERENTIAL WITH CAPACITIVE CROSS COUPLING NEUTRALIZATION

Although differential configuration could reduce the transistor size, but it is not sufficient. Hence, an injection locked LC tank oscillator composing of complementary cross coupled pair (M1-M4) that shown in Fig. 2 is employed to decrease the transistor size more than conventional configuration. The negative resistance which is produced by complimentary CMOS cross coupled could compensate the inductor loss [14].

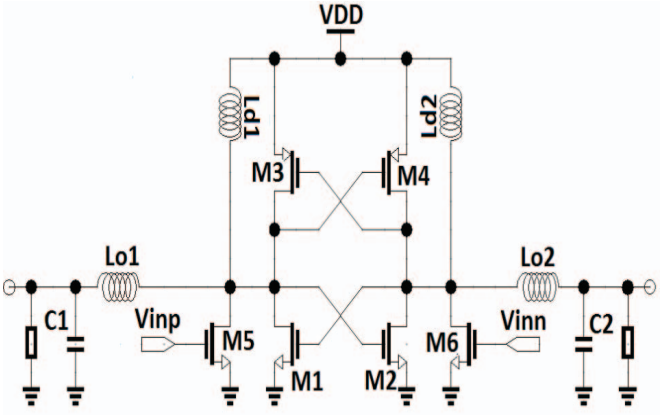


Figure. 2. Differential class-E power amplifier with complementary CMOS cross-pair

The half-circuit equivalent circuit modeled of LC tank oscillator [27] connected to the output of the PA is shown in Fig. 3.

$$\frac{1}{R_{active}} = \frac{1}{R_{m1,2}} + \frac{1}{R_{m3,4}} \tag{7}$$

$$\frac{1}{R_T} = \frac{1}{R_{o1,2}} + \frac{1}{R_{o3,4}} + \frac{1}{R_{o5,6}} + \frac{1}{R_p} + \frac{R_s}{(L\omega)^2} \tag{8}$$

$$C_T = C_{NMOS} + C_{PMOS} + C_P + C_S \tag{9}$$

$$C_{NMOS} = C_{gs1,2} + C_{db5,6} + C_{db1,2} + 2(C_{gd5,6} + C_{gd1,2}) \tag{10}$$

$$C_{PMOS} = C_{gs3,4} + C_{db3,4} + 2C_{gd3,4} \tag{11}$$

Cs, Cp and Rs, RP in 7-11 equations are parasitic elements of the symmetric spiral inductor model [28] of Ld1, 2 shown in Fig. 4.

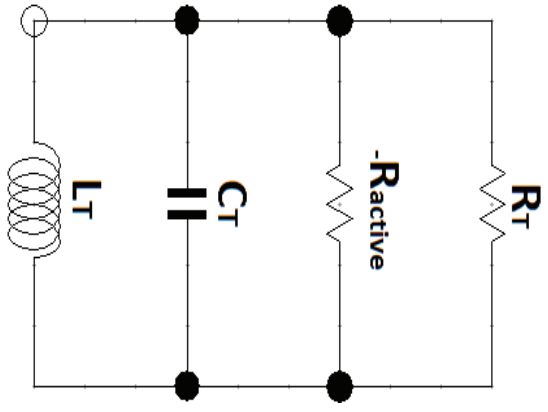


Fig. 3. The equivalent circuit of the LC tank oscillator composed of complementary CMOS cross-coupled pair

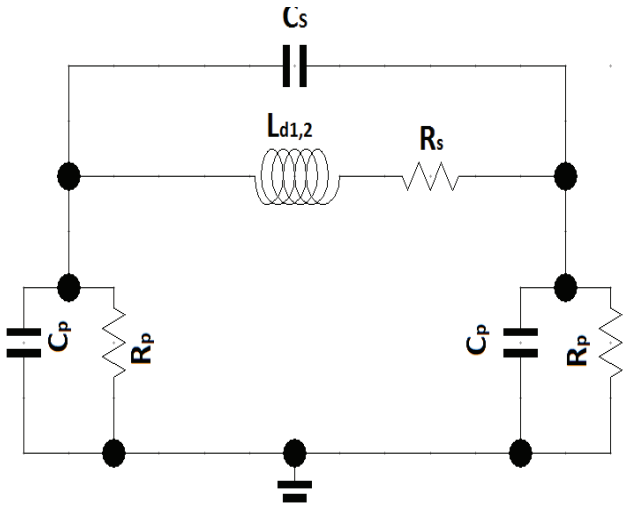
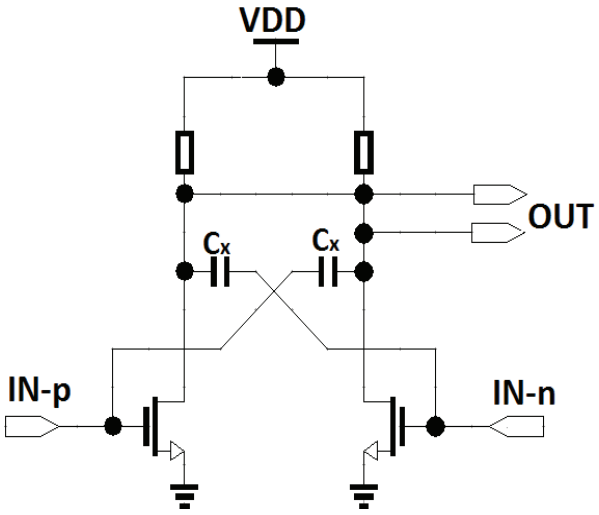


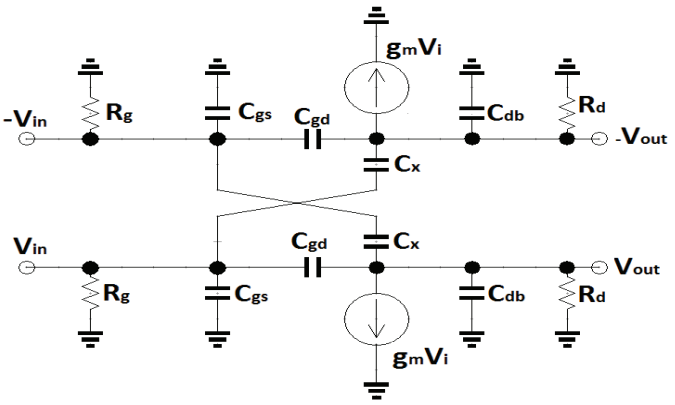
Fig. 4. Symmetric spiral inductor model of Ld1, 2

Current consumption of power transistor reduces outstandingly, because the output operates at the same frequency of input signal frequency by tuning LC tank parameters. Furthermore, the negative conductance of complimentary CMOS cross coupled pair could help to eliminate the power consumption of the inductor $L_{d1,2}$[14]. Stability of this technique is verified by [29].

During high frequency operation, low reverse isolation is one of the most important issues. Parasitic gate to drain capacitance is enormously large due to the large size of PA transistor. The capacitance has an effect on the reverse isolation, power gain and stability. Fig.5 (a) shows a simplified circuit to clarify the capacitance cross coupling neutralization [29]. It is shown that cross coupled (Cx) that settle between the drain and gate of transistor is equivalent to (-Cx). So, parasitic capacitance is neutralized and the reverse isolation is improved.



a. Capacitive cross-coupling neutralization



b. Small signal equivalent circuit of CCC

Fig. 5. Capacitive cross-coupling neutralization circuit schematic

$$Y_{11} = \frac{1}{R_G} + j\omega C_{GS} + j\omega\left(C_{GD} + C_{1,2}\right) \tag{12}$$

$$Y_{12} = -j\omega\left(C_{GD} - C_{1,2}\right) \tag{13}$$

$$Y_{21} = g_m - j\omega\left(C_{GD} - C_{1,2}\right) \tag{14}$$

$$Y_{22} = \frac{1}{R_D} + j\omega C_{DB} + j\omega\left(C_{GD} + C_{1,2}\right) \tag{15}$$

Equation (13) is shown that the effective gate drain transistor could be decreased by using cross coupled capacitor. However, the maximum available gain of PA could be achieve as:

$$G_{MAX} = \left|\frac{Y_{21}}{Y_{12}}\right| = \frac{\sqrt{\omega^2\left(C_{GD} - C_{1,2}\right)^2 + g_m^2}}{\omega\left|C_{GD} - C_{1,2}\right|} \tag{16}$$

This equation conform that cross coupling capacitor could increase the gain.

Now by inspired of the power amplifier introduced in [14, 22], we present a novel class E power amplifier that improve PAE, linearity, Pout and power dissipation in 2.4 GHz in expense of increase area. Proposed PA is shown in Fig. 6.

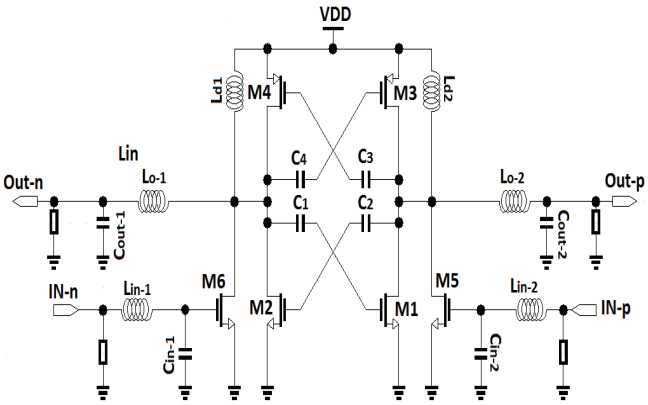


Fig. 6. The proposed differential class-E power amplifier with complementary CMOS cross-pair and Capacitive cross-coupling neutralization

IV. SIMULATION RESULT

The simulation of the proposed PA is performed by 0.18µm CMOS technology of TSMC. The values of used supply voltages and bias currents as well as the aspect ratios of the utilized transistors are optimized for best values of the aimed parameters including the sufficient robustness.

The simulated Pout and PAE versus PIN and frequency are plotted in Fig. 7 and Fig. 8, respectively. This simulation result verified that this structure could achieve 43.6% PAE peak in 2.4GHz and near 1 watt pout. All of this outstanding result are obtained 220mw power consumed.

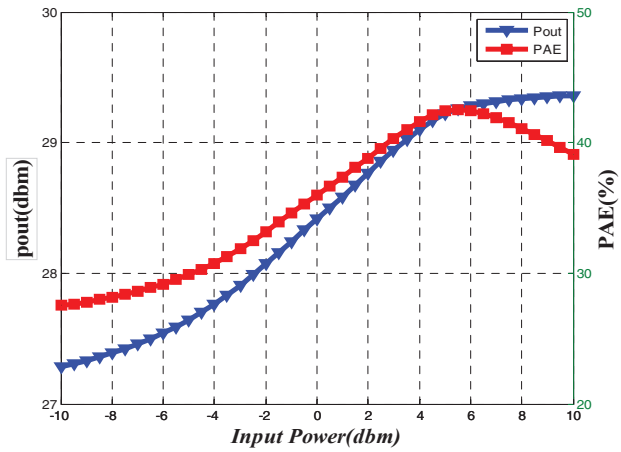


Fig. 7. Simulated output power (dBm), and PAE versus input power.

Finally, to compare the performance of this study against state-of-the-art CMOS PAs, we used the figure of merit (FOM) introduced by the International Technology Roadmap for Semiconductor (ITRS), which normalizes major performances such as output power (Pout), PAE, power gain (G), and the square of operating frequency

$$FOM_{PA} = P_{OUT}.PAE.G.f_0^2 \tag{17}$$

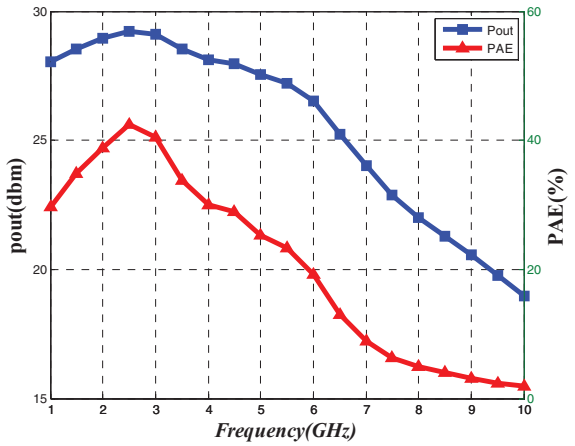


Fig. 8. Simulated output power (dBm), and PAE versus operating frequency.

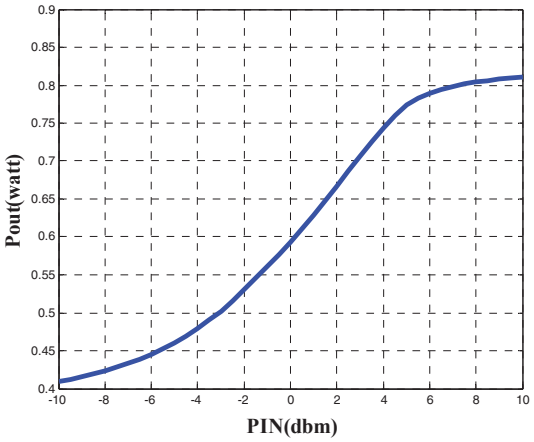


Fig. 9. Simulated power output (watt) versus input power.

Fig. 9, 10 shows the output power of proposed PA versus PIN and frequency, respectively.

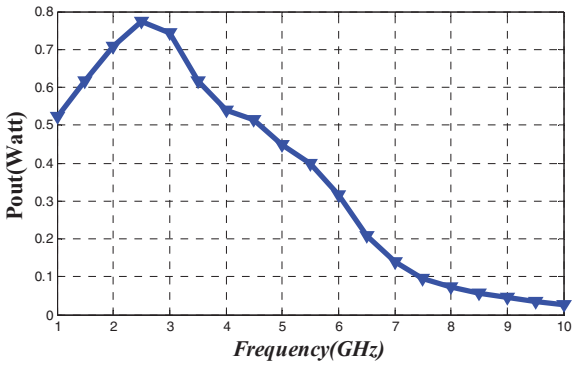


Fig. 10. Simulated power output (watt) versus frequency.

That is the best achievement of this work compared to its advanced matches as is shown in table1.

V. CONCLUSION

In this paper, we presented a differential class-E PA, including capacitive cross-coupling neutralization technique for surplus capacitance on the drain of a class-E amplifier in order to achieve high efficiency. In this technique a differential structure is used to enhance the gain of PA and cross coupling is applied to improve frequency response of PA. This amplifier delivers 28.5-dBm output power with 45% DE and 44% PAE at 2.4 GHz using the 0.18um standard CMOS process. In addition, this work is compare with several other similar paper and shown that it has better performance.

TABLE I. COMPARISON OF STATE OF THE ART CMOS PA

Ref	Tech[um]	Freq[GHz]	V_{DD}[v]	P_{out}[dBm]	PAE[%]	Power[mw]	FOM
[2]	0.18	2.4	1.8	21.5	57	--	--
[8]	0.045	29	1.2	24.5	29	--	--
[14]	0.18	5.7	18	25	42.6	--	--
[23]	0.8	0.824	2.5	32	42	--	24
[24]	0.35	1.9	2	30	48	--	40
[26]	0.13	1.7	2.8	23	67	--	29
[30]	0.35	0.7	2.2	29.5	62	--	--
[31]	0.25	0.9	1.8	29.5	41	--	38
[32]	0.13	1.8	3.5	31.5	51	--	50
[33]	0.13	2.4	2.5	31	58	--	45
This work	0.18	2.4	1.8	28	43	228	73

REFERENCES

[1] H. S. Ruiz and R. B. Pérez, Linear CMOS RF Power Amplifiers: Springer, 2013.

[2] R. Meshkin, A. Saberkari, and M. Niaboli-Guilani, "A novel 2.4 GHz CMOS class-E power amplifier with efficient power control for wireless communications," in Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on, 2010, pp. 599-602.

[3] N. Kumar, C. Prakash, A. Grebennikov, and A. Mediano, "High-efficiency broadband parallel-circuit class E RF power amplifier with reactance-compensation technique," Microwave Theory and Techniques, IEEE Transactions on, vol. 56, pp. 604-612, 2008.

[4] M. K. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," Circuits and Systems, IEEE Transactions on, vol. 34, pp. 149-159, 1987.

[5] A. Grebennikov, "Class E high-efficiency power amplifiers: Historical aspect and future prospect," Applied Microwave and Wireless, vol. 14, p. 64, 2002.

[6] C.-H. Li and Y.-O. Yam, "Maximum frequency and optimum performance of class E power amplifiers," IEE Proceedings-Circuits, Devices and Systems, vol. 141, pp. 174-184, 1994.

[7] X. Du, J. Nan, W. Chen, and Z. Shao, "'New'solutions of Class-E power amplifier with finite dc feed inductor at any duty ratio," Circuits, Devices & Systems, IET, vol. 8, pp. 311-321, 2014.

[8] J. A. Jayamon, J. F. Buckwalter, and P. M. Asbeck, "28 GHz &# 62; 250 mW CMOS Power Amplifier Using Multigate-Cell Design," in Compound Semiconductor Integrated Circuit Symposium (CSICS), 2015 IEEE, 2015, pp. 1-4.

[9] K. Narendra and T. YewKok, "Optimised high-efficiency Class E radio frequency power amplifier for wide bandwidth and high harmonics suppression," IET Circuits, Devices & Systems, vol. 8, pp. 82-89, 2014.

[10] S. Jee, J. Moon, J. Kim, J. Son, and B. Kim, "Switching behavior of class-E power amplifier and its operation above maximum frequency," Microwave Theory and Techniques, IEEE Transactions on, vol. 60, pp. 89-98, 2012.

[11] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," Power Electronics, IEEE Transactions on, vol. 28, pp. 5222-5232, 2013.

[12] P. Alinikula, K. Choi, and S. Long, "Design of class E power amplifier with nonlinear parasitic output capacitance," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, vol. 46, pp. 114-119, 1999.

[13] A. Mediano, P. Molina-Gaudó, and C. Bernal, "Design of class E amplifier with nonlinear and linear shunt capacitances for any duty cycle," Microwave Theory and Techniques, IEEE Transactions on, vol. 55, pp. 484-492, 2007.

[14] P. Heydari and Y. Zhang, "A novel high frequency, high-efficiency, differential class-E power amplifier in 0.18 μm CMOS," in Proceedings of the 2003 international symposium on Low power electronics and design, 2003, pp. 455-458.

[15] M. Iwadare, S. Mori, and K. Ikeda, "Even harmonic resonant class E tuned power amplifier without RF choke," Electronics and Communications in Japan (Part I: Communications), vol. 79, pp. 23-30, 1996.

[16] C. P. Avratoglou and N. C. Voulgaris, "A class E tuned amplifier configuration with finite DC-feed inductance and no capacitance in parallel with switch," Circuits and Systems, IEEE Transactions on, vol. 35, pp. 416-422, 1988.

[17] A. V. Grebennikov and H. Jaeger, "Class E with parallel circuit-a new challenge for high-efficiency RF and microwave power amplifiers," in Microwave Symposium Digest, 2002 IEEE MTT-S International, 2002, pp. 1627-1630.

[18] A. Grebennikov, "Load network design techniques for class E RF and microwave amplifiers," High Frequency Electronics, vol. 3, pp. 18-32, 2004.

[19] J. Y. Hasani and M. Kamarei, "Analysis and optimum design of a class E RF power amplifier," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 55, pp. 1759-1768, 2008.

[20] A. J. Wilkinson and J. K. Everard, "Transmission-line load-network topology for class-E power amplifiers," Microwave Theory and Techniques, IEEE Transactions on, vol. 49, pp. 1202-1210, 2001.

[21] W. Zhuo, X. Li, S. Shekhar, S. Embabi, D. Gyvez, J. Pineda, et al., "A capacitor cross-coupled common-gate low-noise amplifier," Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 52, pp. 875-879, 2005.

[22] H. Asada, K. Matsushita, K. Bunsen, K. Okada, and A. Matsuzawa, "A 60GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16% PAE," in Microwave Conference (EuMC), 2011 41st European, 2011, pp. 1115-1118.

[23] D. Su and W. McFarland, "A 2.5-V, 1-W monolithic CMOS RF power amplifier," in Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997, 1997, pp. 189-192.

[24] K.-C. Tsai and P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," Solid-State Circuits, IEEE Journal of, vol. 34, pp. 962-970, 1999.

[25] R. Brama, L. Larcher, A. Mazzanti, and F. Svelto, "A 30.5 dBm 48% PAE CMOS class-E PA with integrated balun for RF applications," Solid-State Circuits, IEEE Journal of, vol. 43, pp. 1755-1762, 2008.

[26] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "Analysis of reliability and power efficiency in cascode class-E PAs," Solid-State Circuits, IEEE Journal of, vol. 41, pp. 1222-1229, 2006.

[27] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," Solid-State Circuits, IEEE Journal of, vol. 34, pp. 717-724, 1999.

[28] C. P. Yu, C. Ryu, J. Lau, T. H. Lee, and S. Wong, "A physical model for planar spiral inductors on silicon," in International electron devices meeting, 1996, pp. 155-158.

[29] W. L. Chan, J. R. Long, M. Spirito, and J. J. Pekarik, "A 60GHz-band 1V 11.5 dBm power amplifier with 11% PAE in 65nm CMOS," in Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, 2009, pp. 380-381,381 a.

[30] K. L. Mertens and M. S. Steyaert, "A 700-MHz 1-W fully differential CMOS class-E power amplifier," Solid-State Circuits, IEEE Journal of, vol. 37, pp. 137-141, 2002.

[31] C. Yoo and Q. Huang, "A common-gate switched 0.9-W class-E power amplifier with 41% PAE in 0.25-μm CMOS," Solid-State Circuits, IEEE Journal of, vol. 36, pp. 823-830, 2001.

[32] Y. Song, S. Lee, E. Cho, J. Lee, and S. Nam, "A CMOS class-E power amplifier with voltage stress relief and enhanced efficiency," Microwave Theory and Techniques, IEEE Transactions on, vol. 58, pp. 310-317, 2010.

[33] R. Brama, L. Larcher, A. Mazzanti and F. Svelto, "A 1.7-GHz 31dBm differential CMOS class-E power amplifier with 58% PAE," Costom Integrated Circuits Conference, pp. 551-554, Sept. 2007.