A 3.48ps Jitter @ 1.45GHz Fully Differential Dual band DCO with a new Reconfigurable Delay Cell

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Abstract— In this paper a dual band differential Digital-Controlled-Oscillator (DCO) with a reconfigurable delay cell in each four stages of digitally controlled ring Oscillator is proposed. The bands switching will done by a digital mode select bit. Each band will controls by 6 bit codes and varies in a 50MHz band width. Band variations occurs by changing the sizing of the current tails of Source-Coupled-Logic (SCL) based delay cells. A new SCL based delay cell is used which has a reconfigurable structure. The structure transformation influence on power and delay path. But in each band the power consumption profile has a monotonic changes. Fully differential oriented structure ensures low jitter design, 6.04ps @505.1MHz in lower band and for upper band 3.48ps @1.45MHz. The simulations are in 180nm CMOS technology. First band with select bit 0 has frequency range [455.2-505.1] MHz and consumes power 1.98mW @455MHz. Upper band in select bit 1 position with frequency range of [1.39-1.45] MHz has power consumption , 9.7mW @1.39GHz. Small signal model for delay calculation and circuit analysis are done for validity of results. Also, Monte Carlo and central frequency disturbance are shown the acceptable operation of the proposed circuit.

Keywords: *Dual band; Digital-Controlled-Oscillator (DCO); Reconfigurable; Digital select bit; Source- Coupled- Logic (SCL); Fully Differential; Monte Carlo.*

I. INTRODUCTION

Dual band PLL circuits are familiar concept for multi band communication standards. They can be used as a single LO (local oscillator) but oscillating at different frequencies with separate bands. First dual band VCOs are high frequency LC tanks with high occupied area which a switch change the involve inductors and the output frequency band switches [1]. Some other multi band PLL are switching between bands by frequency divider [2]. A multiband frequency synthesizer (PLL based) for several bands for DRM/DRM+/DAB systems based on programmable divider presented in [3]. First dual band ADPLL used for WiMAX based on frequency divider is [4]. In digital controlled PLL domain such as PLL, the DCO (VCO) is the most important unit from aspect of power consumption, up to 90% of system power, area and complexity [5]. Therefore, optimization of DCO can results in overall circuit performance especially power. Dual band ADPLL with dual band RO based DCO architecture is presented by [6]. The DCO has a mode select bit which varies the delay of coarse stage and provides a

few (15MHz) frequency gap between operation bands of DCO. Center frequency and the frequency gap between bands are low and the linearization circuit added up to linear the characteristic of frequency vs. code occupying such a high area. Also the power vs. input frequency diagram has an ascending regime such as expected from the circuit designed in CMOS structure. In this paper a new differential DCO with a mutable delay element stricter by a digital mode select bit is proposed. Design of DCO base on SCL topology lead to an almost uniform changes regime for power vs. frequency in each band. The DCO has a linear f vs. input code with no extra circuit and also provides full swing without any replica bias circuit [7]. Replica bias provides the noise margin for next stage by changing the bias of circuit in analog circuits, such as SCL Ring Oscillators (RO). Differential structure make jitter very low and damp the common noise.

The paper organization is as follows: section 1; introduction, Section 2; circuit descriptions, Section 3 and simulation results, conclusion and results.

II. CERCUIT DESCREIPTIONS

A. DCO structure

The proposed DCO has a RO topology. RO oscillators has wider frequency range, more output phase and on-chip integration capability but more phase noise than LC tank. Therefore our proposed DCO is designed based on four stages of mutable hysteresis delay element based on SCL circuits.

Figure 1 shows the proposed dual band DCO with block diagram of delay elements. These stages are cross connected with 1.8v swings. The differential structure make the jitter of DCO very lower than the same works.

All the stages has 7 control line for digital bits. 6 of them varies the frequency of each band by one hot codes [C5:C0]. One digital bit selects the structure of DCO for working in the lower or upper band, band select bit.

When the band select bit is low (digital 0), the delay element structure has more propagation delay. Therefore the total delay of DCO increases and frequency varies by input codes in lower band [455.2MHz- 505.1MHz]. By changing the band select bit to high (digital 1), the delay of each Schmitt trigger (ST) delay element decrease and DCO works in upper band frequencies [1.39GHz -1.45GHz].
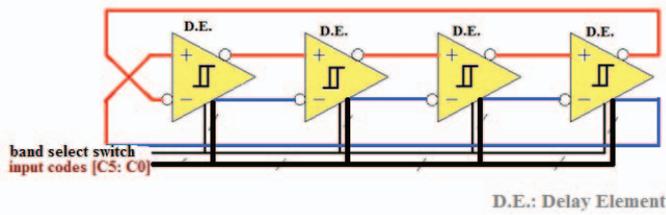
Figure 1. Block diagram of the proposed differential dual band DCO.

Our proposed circuit is designed mainly on 3 basis.
I. Differential and symmetric circuit, ii. Dual band structure and iii. Low power design.

- Increasing the frequency of RO circuit is from two way, decreasing the number of stages which results in lower output sampling phases or delay of each stage, which is depends on internal structure and parasitic capacitance and resistance. Differential design help us to have more output phases with lower number of stages. Therefore the frequency in our proposed circuit is higher than same topologies. Also, jitter and common noise are improved by this approach.

- Dual band structure help the DCO to work in two band with gap about 800MHz with just by a digital bit, in run time of circuit instead of two separate DCO.

- Low power design is main goal of today's circuit designers. There is a direct relationship with increasing frequency and power consumption in CMOS. Using SCL nature in our circuit help us to have more uniform changes of power vs increasing the frequency in each band, will discuss later. Also, in a system when the high frequency is demanded, the higher power and low frequencies consume less power consumption can exchange by mode bit.

B. Schmitt trigger delay structre

The delay element used in our DCO is a Schmitt Trigger mutable SCL based fully differential element, Figure 2. Delay element composes from two differential SCL inverter. A feedback and two band select switches. The delay element has a hysteresis in its characteristic because it causes the transient of pulses reduce and lower the power consumption. The hysteresis is formed by a positive feedback from second SCL inverter to first one. The feedback eliminates when the DCO select to work at lower band. Therefore the delay of this element increases and the frequency decreases to lower band. The band select switches are simple NMOS transistors their gate controls by a digital bit. Input codes [C5: C0] apply to current source of each SCL inverter. Figure 3, shows the circuit schematic of delay element. Each SCL inverter has transistors as current tails. These transistor gates are control by input codes. Each tail has 6 NMOS. The tails are sized so that the characteristic of frequency vs. input codes be linear. Each SCL inverter has 5 transistors, two PMOSs as load and one NMOS as tail. The cross coupled PMOS loads provides full swing especially when the feedback influences on noise margin of next stage input signals (second SCL inverter). Otherwise the replica bias should be used. The inputs signals apply to $M_{1, 2}$.
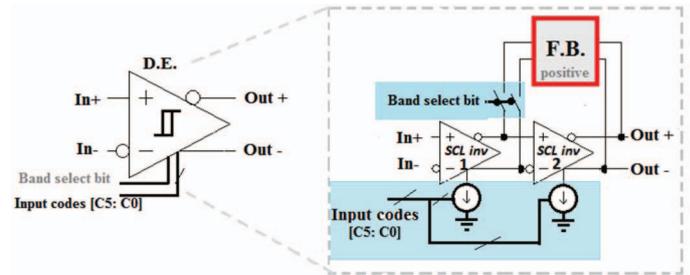

Figure 2. Block diagram of differential mutable delay element.
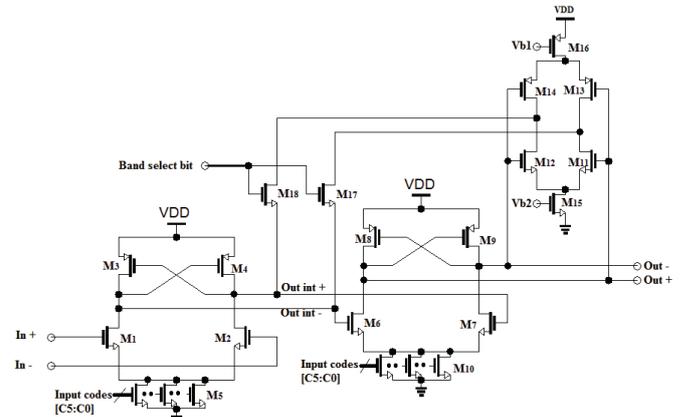

Figure 3. Differential delay element circuit.

By choosing the frequency (C5:C0) and band (band select bit) the first SCL inverter make intermediate signal out int. the intermediate outputs make the next SCL inverter inputs. The feedback is an SCL based which the current tails $M_{15, 16}$ controls its delay. Positive feedback in addition to make the "In" to "Out" signals delay shorter, Make a hysteresis to reduce signals transitions in high frequencies such as GHz. Also, this SCL based structure will keep the power changes vs. frequency in each band (not both, because of structure change in bands) almost stationary, Figure 4. Figure 5 illustrates the DCO bands. The bands are linear with no extra circuit and has band gap about 800MHz. Each band with is equal to 50MHz, more than same works. Figure 6, shows comparison of dual band DCO of proposed and same RO based structure. Figure 6 shows that the band widths, band gap, central frequencies of proposed DCO are improved than same dual band DCOs.
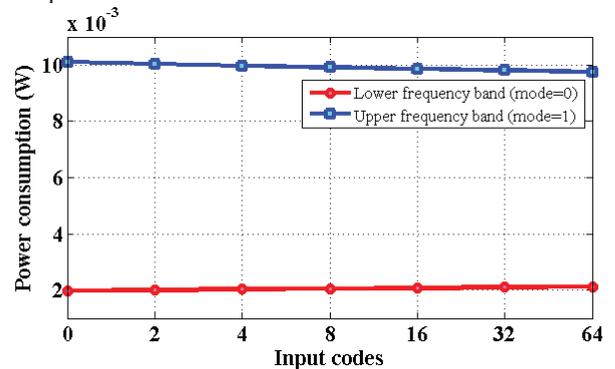

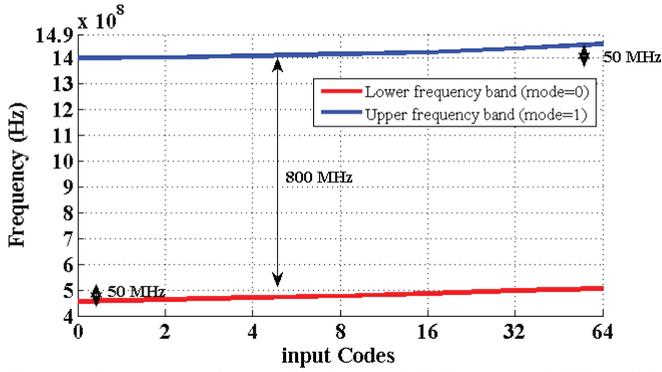Figure 4. Power vs. input codes characteristic for proposed differential dual band DCO.

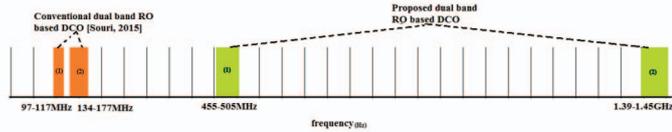Figure 5. Frequency vs. input codes characteristic for proposed differential dual band DCO.

Figure 6. The band comparison of proposed dual band and conventional dual band DCO [6].

Using small signal model of transistors and the symmetric differential structure of proposed delay element, we obtain the approximately model and delay equations of DCO. We assumes that the switches ideal and wire connected because has no special effect on delay. Using half circuit and placement of small signal model in each transistor of Figure 3, and (1) we reach to equal small signal model shown in Figure 7.

$$c_1 = c_{gb2} + c_{gs2} \quad (1)$$
$$g_{mi} = g_{m2}$$
$$g_{mii} = g_{m7}$$
$$c_f = c_{gd7}$$
$$c_{out} = c_{db7}$$
$$R_{mid} = r_{o2} \| r_{o8} \| 1/g_{m3}$$

V_x is drain voltage of M_2

Transfer function of circuit Figure 7 is shown in (2).

$$H(s) = \frac{-(C_{out}R_{out}s + 1)(g_{mii} - C_f s)(g_{m1} - C_{gd1}s)(g_{mf} - C_f s + C_{mid}s + C_{mid}g_{mf}R_{in}s - C_f C_{mid}R_{in}S^2)}{s(C_{mid}R_{in}s + 1)(C_f + C_{out} + C_f C_{out}R_{out}s)}$$

(2)

Using ailoto [8] method for delay approximate equation. We use the pole of function (2). The dominant pole which determines the delay approximately. By replacing natural frequency s with $j2\pi f$, the propagation delay of delay element is inversely proportion to dominant pole of (2) as shown in (3). $C_{db12} + C_{db14}$ are the elements from feedback which eliminates in lower band frequencies. Therefore, the band1 delay equation is as (4). Comparison of (3, 4) shows that frequency at band 2 would be higher than band1 due to feedback.

$$\tau_{p,band2} = \frac{C_{mid}R_{in}}{2\pi} \approx \quad (3)$$
$$\frac{(C_{gb5} + C_{gs5} + C_{db3} + C_{db1} + C_{db12} + C_{db14})(-\frac{1}{g_{m3}})}{2\pi}$$

$$\tau_{p,band1} = \frac{C_{mid}R_{in}}{2\pi} \approx \frac{(C_{gb5} + C_{gs5} + C_{db3} + C_{db1} +)(-\frac{1}{g_{m3}})}{2\pi} \quad (4)$$

The comparison of proposed dual band DCO with other works is discussed in TABLE 1.
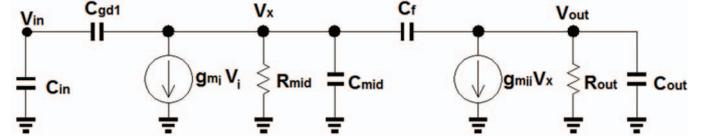

Figure 7. The band comparison of proposed dual band and conventional dual band DCO.

TABLE 1. PROPOSED DCO COMPARE AND REVISION.

	Proposed DCO		[6]		[9]	[10]
Tech. (nm)	180		180		180	180
Supply voltage (V)	1.8		1.8		1.8	1.8
DCO control bit	6 bit+1 mode select bit		6 bit+1 mode select bit		15	6 bit
Num. of bands	Dual band		Dual band		Single band	Single band
Num. of stage/ phase	4/8		10+1MUX+1NOR enable/ 11		32/32	5/5
	SCL mode	*ST mode*	*SCL mode*	*ST mode*		
Frequency range	455.2MHz~505.1MHz	1.39GHz~1.452GHz	97.18MHz~117.65MHz	134.05MHz~177.03MHz	205 MHz~925MHz	4MHz~416MHz
Band width (MHz)	50	50	20.47	42.98	720	412
Band Gap (MHz)	884.9		16.4		-	-
Jitter (P2P)	6.04ps	3.48ps	14.8ps		90ps	N.R*
Power	1.98mW @455 MHz	9.7mW @1.39 GHz	1.37mW @134M Hz	1.78mW @137.3 MHz	255uW @205MHz	N.R

N.R*: Not Reported

III. SIMULATIONS AND RESULTS

The proposed circuit validity is tested by PVT and jitter Monte Carlo analysis. The peak to peak jitter is measured by 500 Monte Carlo runs. Jitter is lower than the other references and same work, that's due to differential and symmetric structure. The frequency variation around the central frequency is shown in Figure 9. It shown frequency stability with temperature variation compares with other dual band DCOs. Figure 10 also shows process variation of frequency vs. input codes.

The simulation shows the validity of proposed circuit performance. The proposed DCO design for two band work with steady power regime in compare with frequency changes in each band the frequency of DCO is higher than conventional works.
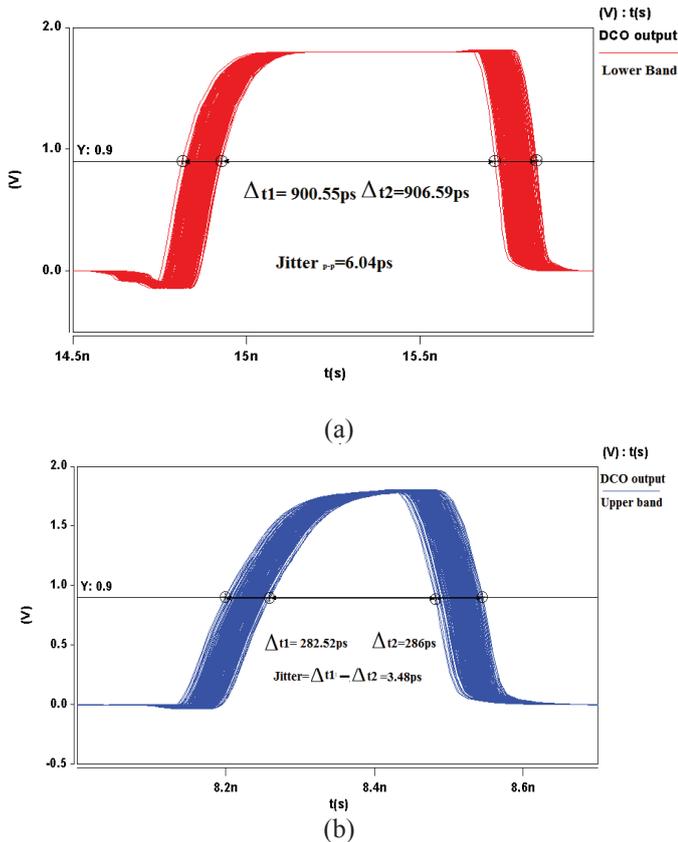
(a)

(b)

Figure 8. Time-period jitter of the proposed DCO (Monte Carlo analysis). (a) Lower band jitter 6.04ps @ 505.1MHz. (b) Upper band 3.48ps @ 1.45GHz.

DCO in lower (455.2~505.1MHz) consumes less power (1.98mW~2.12mW) and its frequency step is gap to next band is about 884MHz. The upper band with frequency range of (1.39~1.452GHz) consumes more power (9.7mW ~10.1mW). The power change in each band is almost independent from frequency because of SCL based circuit characteristic. Peak to peak jitter for bands are 6.04ps @ 505.1MHz and 3.48ps @ 1.45GHz, respectively. The simulation results shows operation validity of the proposed design.
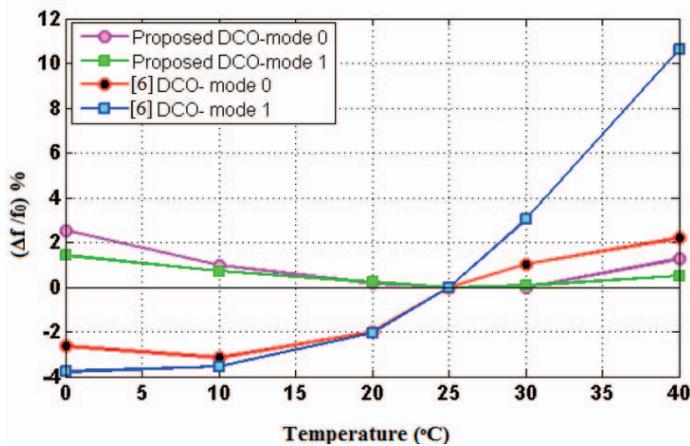

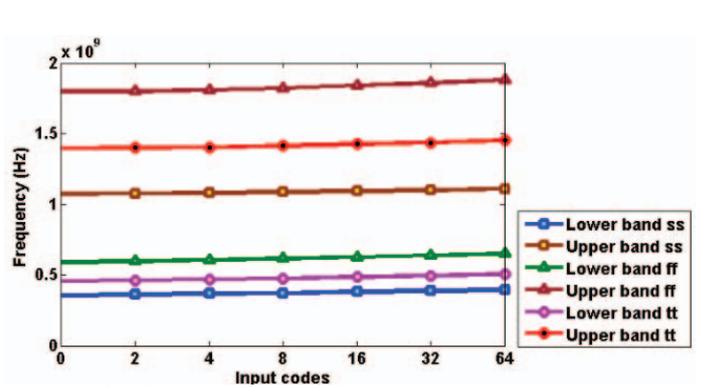Figure 9. Comparison of a $\Delta f / f0$ parameter for proposed DCO and [6].

Figure 10. Frequency characteristic vs. input codes corner analysis in proposed dual band DCO.

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