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Graphene nanoribbon tunnel field effect transistor with lightly doped drain: Numerical simulations

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ABSTRACT

By inserting a lightly doped region between the highly doped drain and the intrinsic channel of a graphene nanoribbon tunnel field effect transistor (GNR-TFET), we propose a new lightly doped drain (LDD)-GNR-TFET. Transport characteristics of the proposed transistor is numerically simulated, employing the third-nearest-neighbor tight-binding approximation in mode space non-equilibrium Green's function formulism (NEGF), in ballistic regime. Simulations show, in comparison with a conventional GNR-TFET of the same dimensions, the proposed LDD-GNR-TFET exhibits a 10^2–10^3 times smaller OFF-current, an up to 10^5 times larger ON/OFF ratio, a shorter time delay, a smaller power-delay product (PDP) and a less drain induced barrier thinning (DIBT), besides preserving the subthreshold swing.

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1. Introduction

Graphene, due to its superior electrical, thermal, and mechanical properties [1–3] and its stripes known as graphene nano ribbons (GNRs) [4–9] are theoretically and experimentally shown to be potential candidates to substitute for Si in electronic industry. It has been demonstrated that only semiconducting armchair GNRs (A-GNRs) with band gaps of 10-nm wide and narrower are suitable for electronic and optoelectronic device applications.

Experimental and theoretical studies show that GNR field effect transistors (GNR-FETs) [10–16] and GNR Tunnel FETs (GNR-TFETs) [17–21] with sub-10 nm GNR channels can achieve ON/OFF ratios higher than 10^6, and sub-threshold slopes much smaller than the theoretical limit of 60 mV/dec for MOSFETs. This capability makes them potential candidates for low power applications. A GNR-TFET is a p-i-n type structure, with an intrinsic channel sandwiched between highly doped p^+ and n^+ regions with ohmic contacts, respectively acting as source and drain terminals. This transistor operates under reverse applied biases. The dominant carrier transport mechanism in a GNR-TFET in ON-state is the band to band tunneling (BTBT) from source valence band to the channel conduction band. This is why a GNR-TFET is capable of achieving the reported low sub-threshold swing. Nevertheless, transistors like GNR- and CNT-FETs suffer from ambipolarity in their OFF-states, mainly under negative gate biases. The origin of this behavior is BTBT between the drain conduction band and the source valance band. Ambipolarity is, however, a major drawback that needs to be overcome in these transistors. A few research groups have already proposed various techniques both in GNR-FETs [16] and CNT-FETs [22–24] to reduce the BTBT in their OFF-states and hence overcoming their ambipolarities. Use of uniaxial tensile strain across the channel of a dual gated GNR-FET [16] has shown to improve the device ON/OFF ratio by four orders of magnitudes while decreasing the ON current by up to about two orders of magnitude. Nevertheless, use of appropriate lightly doped and band engineered source and drain regions in CNT-FETs [22–24] have shown to reduce the OFF currents by 3–4 orders of magnitudes, while slightly improving the ON current. Taking advantage of the less troublesome approach of [22], we have proposed to introduce only a single lightly doped (n^-) region between the channel and the drain (n^+) region of a GNR-TFET. The added lightly doped drain (LDD) is expected to widen the tunnel-barrier on the drain-side of the channel, suppressing the direct BTBT between the drain conduction band and source valence band, in the device OFF-state, and hence improving the transistor ambipolar behavior to some degree.

Employing the third-nearest-neighbor tight-binding approximation in the mode space non-equilibrium Green's function formulism (NEGF) and assuming ballistic transport, we have simulated characteristics of the proposed LDD-GNR-TFET. Simulations show significant improvements in the OFF-current, ON/OFF ratio, time delay, power-delay product (PDP) and the drain induced barrier thinning (DIBT) for the LDD-GNR-TFET while preserving the subthreshold swing, in comparison with a conventional GNR-TFET of the same dimensions.

The rest of the paper is organized as follows. In Section 2, the proposed structure is brought forward. The simulation method is explained in Section 3. Then, the simulation results together with supporting discussions are presented in Section 4. Finally, the paper is closed with conclusions in Section 5.

2. Proposed structure

Schematic side views of the structures of (a) conventional dual gated GNR-TFET and (b) the proposed LDD-GNR-TFET together with corresponding relative doping profiles $[N_D(x) - N_A(x)]$ are illustrated in Fig. 1. Each transistor is assumed to be made of a 75-nm long semiconducting armchair GNR with $n = 16$ (i.e., 16-A-GNR), whose width and bandgap are $W = 1.84$ nm and $E_G = 0.7$ eV, respectively. The source (p^+) regions in both transistors and the heavily doped drain region of the conventional GNR-TFET are all taken to be the 30-nm long, respectively doped with $N_{AS} = 10^{-2}$ (acceptors/atom) and $N_{DD} = 10^{-2}$ (donors/atom). The n^--doped LDD region of the proposed structure is assumed to be 15 nm long and doped with donor concentration of $N_{LD} = N_{DD}/16$. In either transistor, the middle 15-nm long intrinsic A-GNR that acts as the channel is assumed be sandwiched between top and bottom insulating gate dielectric layers made of 1.5-nm thick HfO_2 with the relative dielectric constant of $\varepsilon_{ox} = 16$. Each HfO_2 layer is assumed to be topped with a compatible metal layer to act as the gate electrode.

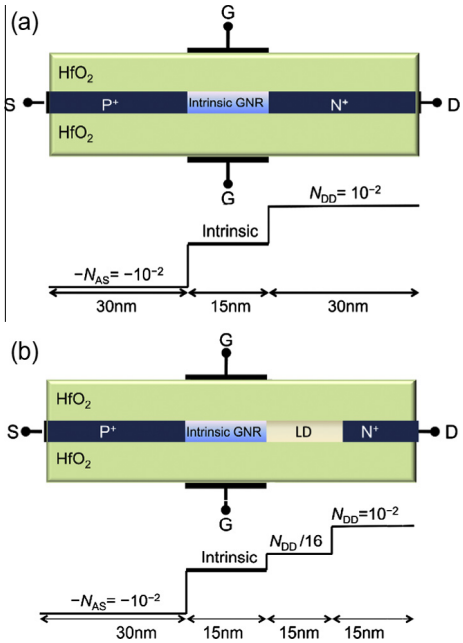

Fig. 1. Schematic side views of the (a) conventional GNR-TFET and (b) proposed LDD-GNR-TFET. The channels are 15-nm long 16-A-GNRs topped with 1.5-nm thick layers of HfO_2 with relative dielectric constant of $\varepsilon_{ox} = 16$.

3. Simulation approach

Self-consistent solution of the mode space non-equilibrium Green's function (NEGF) in the ballistic transport limit, as described in [25–27], with the Poisson's equation is employed to perform the device simulation. As described in [28] the mode space approach with an accuracy of greater than 95% is used to reduce the simulation time and computational cost. Furthermore, for the range of the applied voltages used in this work, inclusion of two subbands for simulating TFETs made of 16-A-GNR is sufficient enough. The foundation of NEGF method is based on the retarded Green's function that is described by:

$$G(E) = [(E + i0^{+})I - H - \Sigma_S - \Sigma_D]^{-1} \tag{1}$$

where E is energy, I and H are the identity and Hamiltonian matrices, and Σ_S and Σ_D are the self-energy matrices, representing the coupling of the channel to the source and the drain contacts, respectively.

In order to compute the retarded Green's function, one should to calculate the Hamiltonian for the isolated channel, using suitable basis functions [28]. Potential distribution obtained from the solution to Poisson's equation is also entered in the NEGF formalism at this stage.

The Hamiltonian matrix of an A-GNR can be calculated by the third-nearest neighbor tight-binding approximation with only one orbital coupling (p_z orbital) as,

$$H = \begin{bmatrix} U_1 & b_2 & 0 & t_3 & & \\ b_2 & U_2 & b_1 & 0 & t_3 & \\ 0 & b_1 & U_3 & b_2 & 0 & \ddots \\ t_3 & 0 & b_2 & U_4 & b_1 & \ddots \\ & t_3 & 0 & b_1 & U_5 & \ddots \\ & & \ddots & \ddots & \ddots & \ddots \end{bmatrix} \tag{2}$$

wherein $U_i (i = 1, 2, 3, \ldots)$ is representing the on-site electrostatic potential at the i-th A-GNR ring,

$$b_1 = t_1 \left\{ 1 + \frac{4C_{\text{edge}}}{(n+1)} \sin^2 \frac{\pi}{(n+1)} \right\}$$

and

$$b_2 = 2t_1 \cos \frac{\pi}{(n+1)}$$

are the hopping parameters between the first and the second nearest neighboring A-GNR rings, respectively, $t_1 \approx 2.7$ and $t_3 \approx 0.2$ eV are the hopping parameters between the first and the third nearest neighboring carbon atoms, and $C_{\text{edge}} = 0.12$ represents the edge bond relaxation. The latter parameter is used to include the A-GNR edge effect into account.

The self-energy matrices can be calculated as described in [28], in details. The Sancho–Rubio iterative method [29] can be beneficial, in reducing the total simulation time.

Having calculated the retarded Green's function (G) and the self-energy matrices, the density of states for the source and the drain that lead us to the total carriers' density can be found:

$$D_{S(D)} = G\Gamma_{S(D)}G^{\dagger} \tag{3}$$

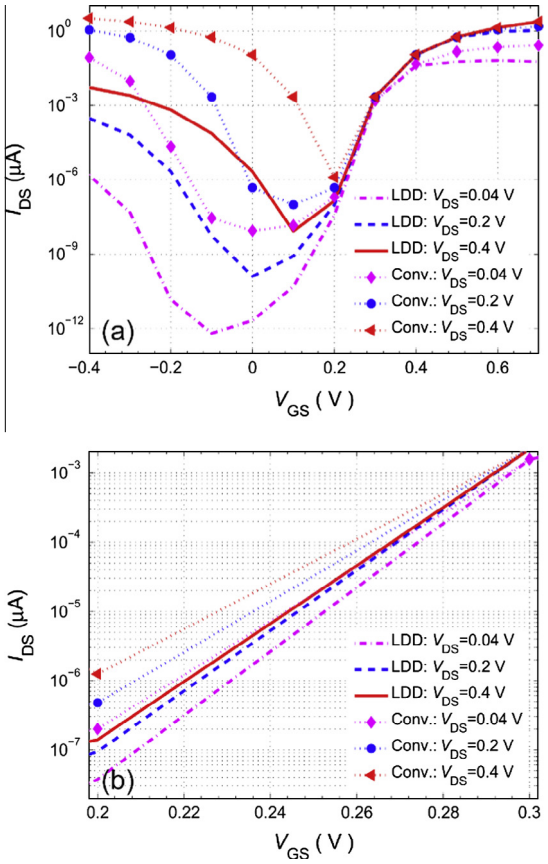

Fig. 2. Comparison of the (a) I_{DS}–V_{GS} characteristics of the proposed LDD-GNR-TFET (lines) with those of and the conventional GNR-TFET (dots with symbols), for $V_{DS} = 0.04$, 0.2, and 0.4 V and (b) zoomed-in portions of the characteristics in the range of $0.2\ \text{V} \leqslant V_{GS} \leqslant 0.3\ \text{V}$.

wherein $\Gamma_{S(D)} = i(\Sigma_{S(D)} - \Sigma^{\dagger}_{S(D)})$ represents broadening of the source (drain) energy levels due to the channel to source (drain) coupling. The resultant total carriers' density in the channel is given by [28],

$$N = \int_{-\infty}^{+\infty} \mathrm{sgn}(E - E_N)\{D_S(E) f[\mathrm{sgn}(E - E_N)\cdot(E - E_{FS})] + D_D(E) f[\mathrm{sgn}(E - E_N)\cdot(E - E_{FD})]\}\, dE \quad (4)$$

where E and E_N are the carriers' energy and the mid gap level of the GNR, respectively, and $f[\mathrm{sgn}(E - E_N)\cdot(E - E_{FS(D)})]$ represents the source (drain) Fermi function corresponding to the Fermi level $E_{FS(D)}$ and $D_{S(D)}$ is the source (drain) density of states. Using Eq. (4) as an input to the Poisson's equation and solving it simultaneously with NEGF in a self consistent manner, the total current flowing across the transistor channel is obtained,

$$I = \frac{2e}{h}\int T(E)[f(E - E_{FS}) - f(E - E_{FD})]\, dE \quad (5)$$

where $T(E) = \mathrm{Trace}(\Gamma_S G \Gamma_D G^{+})$ represents transmission probability of a carrier of energy E between the source and the drain contacts.

4. Results and discussion

The current voltage (I_{DS}–V_{GS}) characteristics of the proposed LDD-GNR-TFET for $V_{DS} = 0.04$ V (dotted-dashes), 0.2 V (dashes) and 0.4 V (solid curve) are illustrated in Fig. 2(a) and are compared

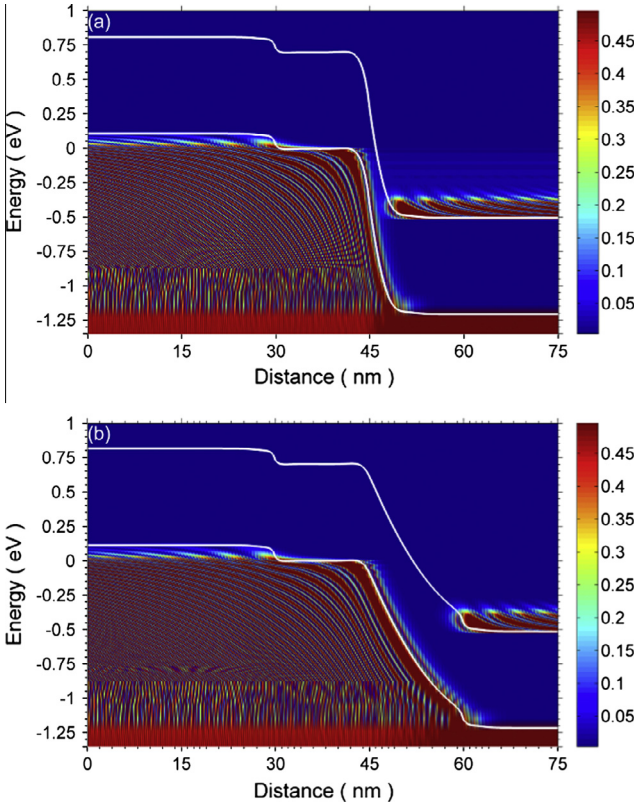

Fig. 3. Comparison of the energy band diagrams (white lines) and the electron density spectrum across the (a) conventional GNR-TFET and (b) LDD-GNR-TFET, both biased in an OFF condition at $V_{DS} = 0.4$ V and $V_{GS} = -0.4$ V. The scale bars on the right indicate the density of electrons.

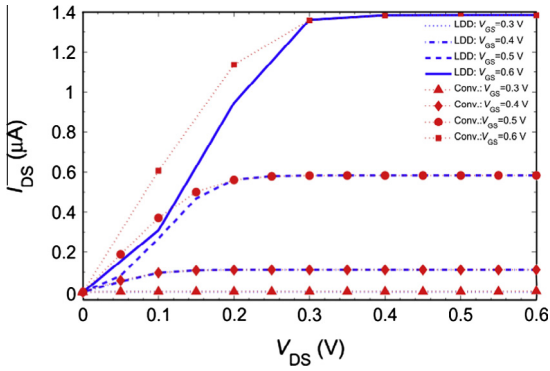

Fig. 4. I_{DS}–V_{DS} characteristics of LDD-GNR-TFET (lines) compared with those of conventional-GNR-TFET (dots and symbols) for V_{GS} = 0.3, 0.4, 0.5, and 0.6 V.

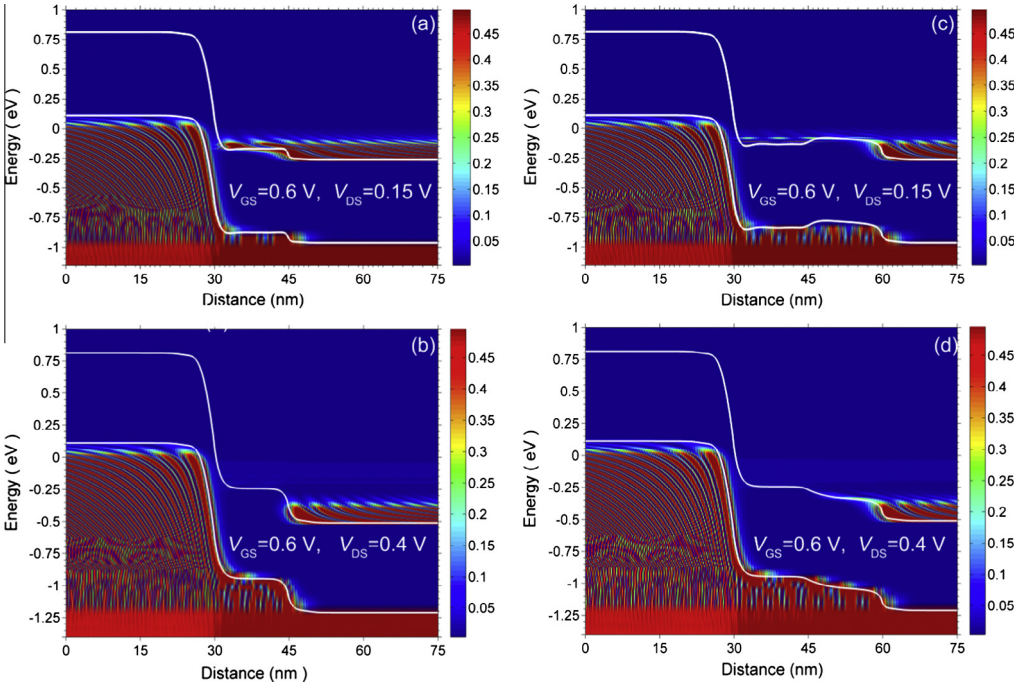

Fig. 5. Comparison of the energy band diagrams (white lines) and the electron density spectrum across the conventional GNR-TFET biased at V_{GS} = 0.6 V and (a) V_{DS} = 0.15 V and (b) V_{DS} = 0.4 V and the proposed LDD-GNR-TFET biased at V_{GS} = 0.6 V and (c) V_{DS} = 0.15 V and (d) V_{DS} = 0.4 V. The scale bars on the right indicate the density of electrons.

with those of the conventional GNR-TFET, under the same biasing condition, depicted by the solid diamond, circles, and triangles , respectively.

As shown in Fig. 2(a), the proposed LDD-GNR-TFET exhibits improved ambipolar behavior that has lowered its OFF currents by almost about three orders of magnitudes in comparison to that of the conventional GNR-TFET, for $V_{GS} = -0.3$ V, and V_{DS} = 0.4 V. All these can be attributed to the presence of lightly doped drain region that widens the tunnel barrier between the channel and the drain, decreasing the probability of the BTBT between the source and the drain, as can be observed in the comparison illustrated in Fig. 3.Fig. 2(b) illustrates zoomed-in portions of the same characteristics depicted in Fig. 2(a), within range of $0.2\ \text{V} \leqslant V_{GS} \leqslant 0.3$ V. This would assist us to evaluate and compare the size of

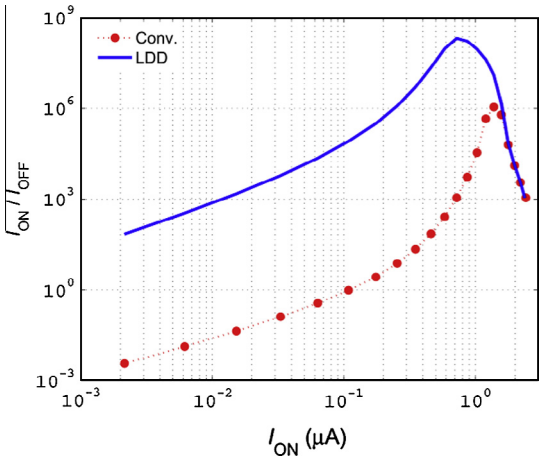

Fig. 6. Comparison between ON/OFF ratios for conventional GNR-TFET (solid circle) and LDD-GNR-TFET (solid line) versus the corresponding ON currents for $V_{DS} = 0.4$ V.

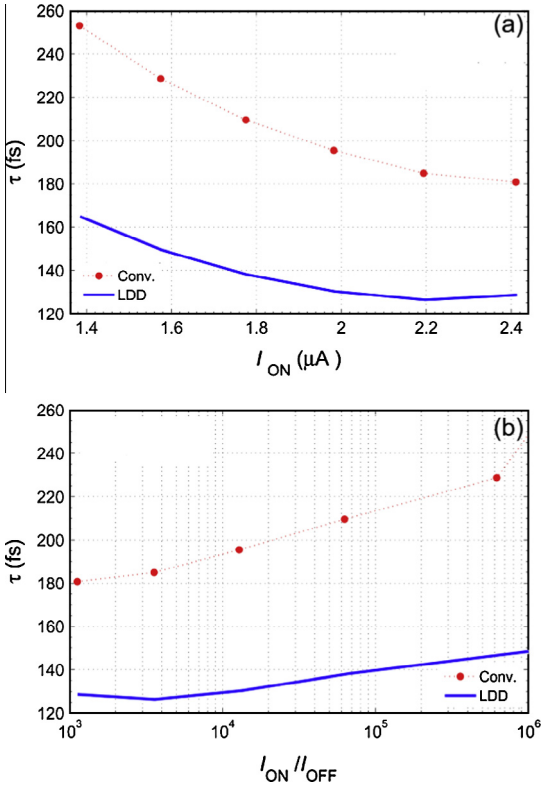

Fig. 7. Comparison of delays time versus (a) ON currents and (b) ON/OFF ratios of the LDD-GNR-TFET (solid lines) and it conventional rival (solid circles) for $V_{DS} = 0.4$ V.

the drain induced barrier thinning (DIBT). On the other hand, the size of DIBT, for any TFET, can be obtained from $\Delta V_{GS}(mV)/\Delta V_{DS}(V)$, for a given current [30]. Comparison of the characteristics of each device biased at V_{DS} = 0.04 and 0.4 V, shows that the size of DIBT for LDD-GNR-TFET at any given current shown in this figure, is smaller than that of the conventional GNR-TFET.

Fig. 3 illustrates the energy band diagrams and the corresponding population per unit energy across both TFETs of Fig. 1, for $V_{GS} = -0.4$ V and $V_{DS} = 0.4$ V. As seen in this comparison the width of the tunnel barrier between the drain and the channel of the LDD-GNR-TFET (Fig. 3(b)) is more than twice as wide as the tunnel barrier in the conventional GNR-TFET (Fig. 3(a)) is. This is why the current traces seen across the barrier in Fig. 3(a) representing the BTBT are not as clear in Fig. 3(b). This is the main cause improvement in the ambipolar behavior of the LDD-GNR-TFET.

To observe and compare the details of the ON currents for both TFETs under study, we have simulated their I_{DS}–V_{DS} characteristics for gate to source biases of V_{GS} = 0.3, 0.4, 0.5, and 0.6 V. The evaluated results are illustrated in Fig. 4. As can be observed from this figure, for V_{GS} larger than threshold values of $V_{TH} \sim 0.3$ V, both devices are turned on. The comparison shows that, except for the triadic region (i.e., $V_{GS} \geqslant 0.4$ V and $V_{DS} \leqslant 0.2$ V), for which the I–V characteristics of the LDD-GNR-TFET exhibit some abnormalities, the differences in the ON currents of the two TFETs under study are insignificant. These can be easily understood by comparing the energy band diagrams and the corresponding population per unit energy across both TFETs biased in two ON-states, as illustrated in Fig. 5, for example with the same V_{GS} = 0.6 V and V_{DS} = 0.15 and 0.4 V.

The band diagrams for the conventional device and its LDD rival with smaller V_{DS} are illustrated in Fig. 5(a) and (c), whereas those for the larger V_{DS} are shown in Fig. 5(b) and (d), respectively. For a given ON-state (i.e., given V_{GS} greater than threshold voltage and $V_{DS} > 0$), in general, a negative electric field that peaks about the source/channel interface, in either TFET, forces the electrons from the

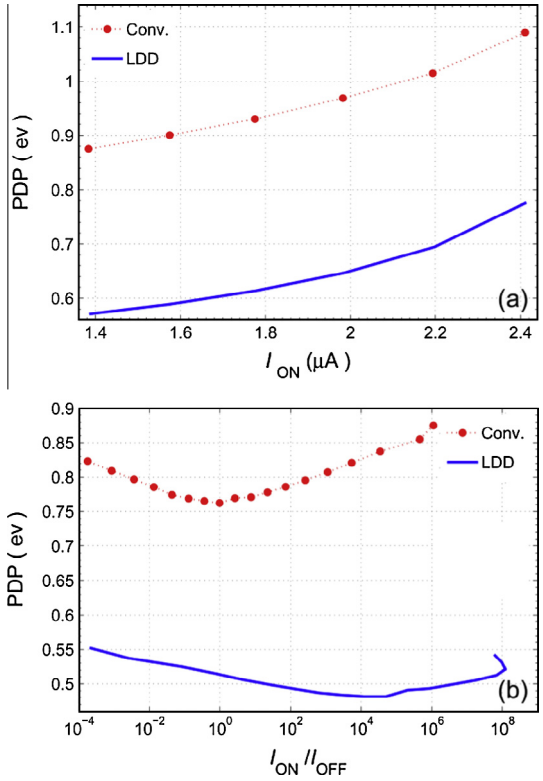

Fig. 8. Comparison of power delay products versus (a) ON currents and (b) ON/OFF ratios of the LDD-GNR-TFET (solid lines) and it conventional rival (solid circles) for V_{DS} = 0.4 V.

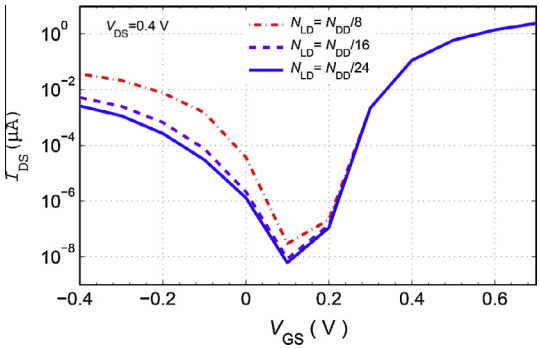

Fig. 9. Comparison between I_{DS}-V_{GS} characteristics of three LDD-GNR-TFETs with lightly doped regions of dopant concentrations $N_{LD} = N_{DD}/8$ (dashes-dots), $N_{DD}/16$ (dashes), and $N_{DD}/24$ (solid line), all biased at $V_{DS} = 0.4$ V.

source valence band to tunnel across a tiny barrier into the corresponding channel conduction band. As seen from Fig. 5(a) and (b), the electrons that have tunneled into the channel of the conventional GNR-TFET, for both biasing conditions, have enough energy to flow into the drain and then out of the device. However, as can be observed from the diagram Fig. 5(c), $V_{DS} = 0.15$ V is not large enough to level the conduction band minima in the LDD region with that of the channel under $V_{GS} = 0.4$ V. Therefore, some of the incoming electrons are confined within the channel and are unable to overcome the LDD barrier, and hence cannot contribute to the drain current. This is the sole reason for aforementioned abnormalities observed in Fig. 4. On the other hand, as seen in Fig. 5(d), size of $V_{DS} = 0.4$ V is large enough to pull the conduction band of the LDD region below that of the channel and let the channel electrons to be fully driven into the drain, contributing to the device saturation.

In order to demonstrate the possibility of using the proposed LDD-GNR-TFET for low power applications, at this point we compare the variation of its ON/OFF ratio versus its ON current at the given drain to source bias of $V_{DS} = 0.4$ V. Fig. 6 illustrates this comparison. In obtaining such variations we have used the same approach as in [31]. As can be observed from this figure, ON/OFF ratio for the LDD-GNR-TFET, in the range of $0.25\ \mu A \leqslant I_{ON} \leqslant 1.4\ \mu A$ is larger than 10^6. Furthermore, the comparison reveals that the ON/OFF ratio for the LDD device, for ON currents in the range of $2\ nA \leqslant I_{ON} \leqslant 0.7\ \mu A$, is almost five orders of magnitudes larger than that of the conventional device.Moreover, we have compared the switching behavior of both structures under study, by evaluating their intrinsic delays (τ) and power-delay products (PDP). In doing so, we used [31]:

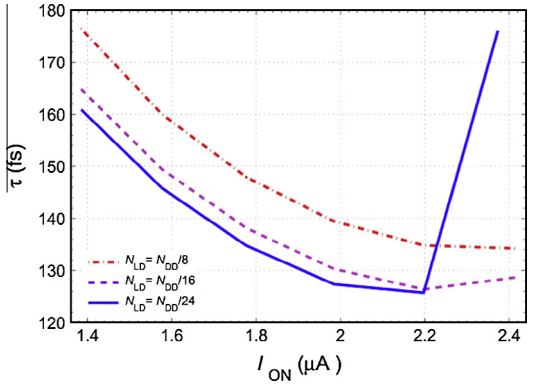

Fig. 10. Comparison between the delay times versus ON-currents of three LDD-GNR-TFETs with lightly doped regions of concentrations $N_{LD} = N_{DD}/8$ (dashes-dots), $N_{DD}/16$ (dashes), and $N_{DD}/24$ (solid line), all biased at $V_{DS} = 0.4$ V.

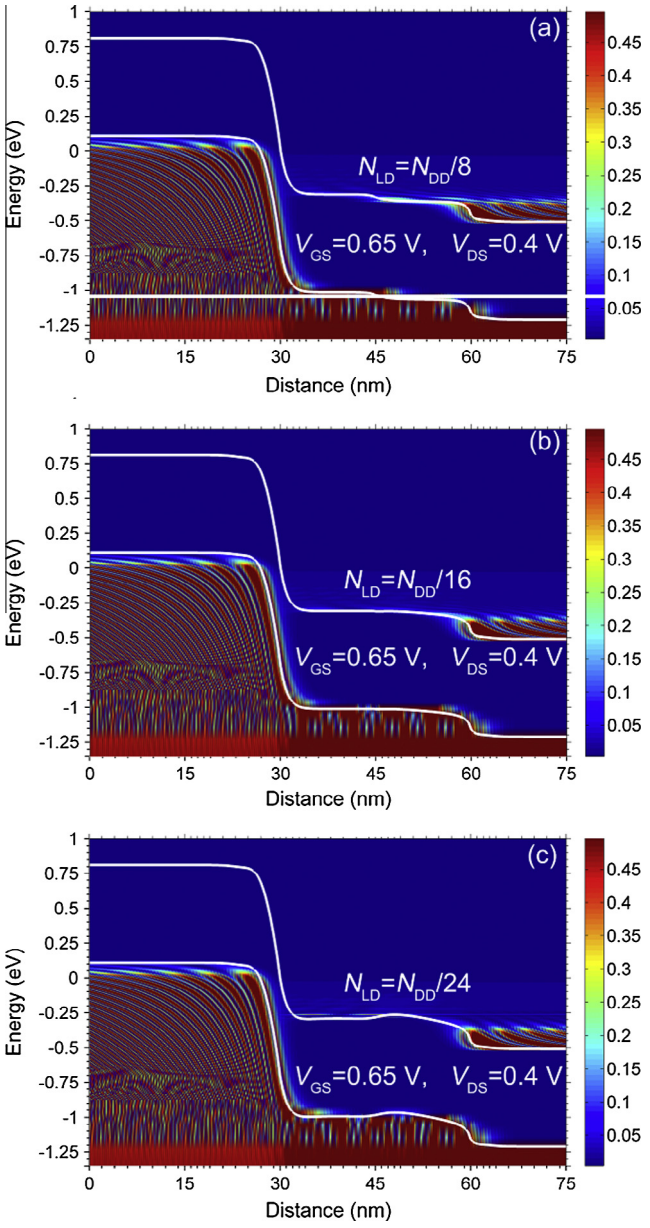

Fig. 11. Comparison of the band diagrams of the three LDD-GNR-TFETs with lightly doped regions of concentrations (a) $N_{LD} = N_{DD}/8$, (b) $N_{LD} = N_{DD}/16$, and (c) $N_{LD} = N_{DD}/24$, all biased at $V_{DS} = 0.4$ V and $V_{GS} = 0.65$ V.

$$\tau = \Delta Q / I_{ON} \tag{6a}$$

$$\Delta Q \equiv (Q_{ON} - Q_{OFF}) \tag{6b}$$

and

$$PDP = \Delta Q \times V_{DD} \tag{7}$$

where Q_{ON} and Q_{OFF} are the total charges in ON- and OFF-states, including the source and the drain regions. Figs. 7 and 8 illustrate the comparisons for τ and PDP versus the corresponding ON currents in the range of 1.4 μA $\leqslant I_{ON} \leqslant$ 2.4 μA, for V_{DS} = 0.4 V, where the ON/OFF ratios, for both devices fall in the range of $10^3 \leqslant I_{ON}/I_{OFF} \leqslant 10^6$. This comparison shows that the switching behavior of the proposed LDD structure is far better than its conventional rival, and hence is more suitable for the low energy consumptions and high speed applications. In fact, use of the lightly doped drain region has reduced the gate to drain parasitic capacitance in the proposed as compared with its conventional rival. As a consequence, the amount of the charge variation, ΔQ, between the gate and the drain contacts of the LDD-GNR-TFET is lower than that in the conventional GNR-TFET. This is the sole reason for the observed improvement in the device switching behavior (i.e., the lower τ and PDP values) for the LDD-GNR-TFET at any given ON current.

So far, we have compared the characteristics of the LDD-GNR-TFET with a low doped region whose dopant concentrations are assumed to be 1/16 of its highly doped drain region with those of its conventional rival. Nonetheless, before performing these comparisons, we had to make sure that the aforementioned dopant concentration is nearly an optimized choice. In doing so, we have first compared the I_{DS}–V_{GS} characteristics of a number of LDD-GNR-TFET with LDD regions of various dopant concentrations, all biased at V_{DS} = 0.4 V. Fig. 9 demonstrates the comparison between the I_{DS}–V_{GS} characteristics for three LDD-GNR-TFET with $N_{LD} = N_{DD}/8$, $N_{DD}/16$, and $N_{DD}/24$, as an example. This comparison, to our expectation, reveals that the smaller the N_{LD} the lower the current below the threshold voltages. This is because as N_{LD} decreases further, the drain carriers in an OFF-state experience an effectively wider tunnel barrier, decreasing the probability of the BTBT mechanism and resulting in an improved ambipolar behavior. However this comparison does not give any information about the possible differences between ON-state characteristics.

To visualize how different these devices can perform in their ON-states, we have evaluated their time-delays versus their corresponding ON-currents ranges wherein their ON/OFF ratios fall in the range of $10^3 \leqslant I_{ON}/I_{OFF} \leqslant 10^6$. Fig. 10, as an example, compares these characteristics for the three devices of Fig. 9, all biased at V_{DS} = 0.4 V.

This comparison shows that for ON-currents $I_{ON} \geqslant$ 2.2 μA the device with smallest N_{LD} experience a sharp linear rise in its delay time. To elaborate more on this issue, we have also compared the band diagrams of the three devices all biased in the same biasing conditions of V_{DS} = 0.4 V and V_{GS} = 0.65 V. Fig. 11 illustrates this comparison. As can be seen from this figure, the bottom of the conduction band in the LDD region of the device with $N_{DD}/24$ has risen above the bottom of the conduction band in the channel region, while those of the one with $N_{DD}/16$ are leveled. Hence, some of the charges in the channel of the former device are trapped and unable to participate in the ON-current, increasing the charge variation, ΔQ, and lowering the ON-current at the same time which in turn results in the sharp rise in the corresponding time-delay as observed in Fig. 10.

5. Conclusion

By introducing a lightly (n) doped region in between the intrinsic channel and the highly (n^+) doped drain region of a p^+-i-n^+ type GNR-TFET, we have proposed a new LDD-GNR-TFET. Simulations show that the proposed device exhibits ON/OFF ratios up to about five orders of magnitudes larger than that of its conventional rival, with similar dimensions. Furthermore, ON state characteristics of the proposed structure, especially subthreshold-swing, are almost unchanged. It has also been demonstrated that the size of the tunnel barrier thinning (DIBT) for the new device is also smaller than that of the conventional one. The switching behavior of the proposed LDD-GNR-TFET has also been shown to be superior to that of its rival.

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