A Wideband CMOS VGA with dB-Linear Gain Based on Active Feedback and Negative Capacitance

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Abstract—**In this paper, a low power and wideband variable gain amplifier (VGA) with dB-linear gain control characteristic is presented. This design contains three stages of differential amplifier. To achieve accurate dB-linear characteristic and broadband response, sub-threshold loads and negative capacitance are employed, respectively. In addition, active feedback structure is utilized to further extend the bandwidth. Implemented in an 180nm CMOS process, simulation results indicate that the proposed VGA achieves a gain control range of 34 dB, which ~25 dB is dB-linear with ±1 dB gain error and 1.1 GHz bandwidth. The power consumption is only 0.7 mW from a 1.8 V supply.**

Keywords—Variable gain amplifier; low power; dB-linear negative capacitance.

I. INTRODUCTION

Variable gain amplifiers (VGA) are an important mostly analog blocks in wireless communication systems. The VGA should provide a reliable output for different amplitudes of input since the received signal comes from different distances. In other words, an amplifier with a large dynamic range is highly required [1]. The VGAs can be categorized under two main groups according to controllability of their gain. First, the overall gain is adjusted by an analog signal while in the second one that is also called PGA (programmable gain amplifier), the gain is controlled by a digital signal [2]. However, PGAs have some drawbacks like requiring relatively large area overhead due to lots of switches as well as limited gain accuracy due to discrete and finite gain steps. So, the analog controlled counterparts are usually preferred [3-4]. The most important specifications of the VGAs are gain, bandwidth, noise and power consumption. But dB-linear gain control characteristic, which means that the gain in dB linearly follows the control voltage is a vital requisite to obtain a large dynamic range along with an independent settling time with respect to input signal power in AGC circuit [4-5], [6]. Because of the intrinsic exponential characteristic of the bipolar transistors, dB-linear VGA design in bipolar technology is easily achievable. Alternatively, the implementation of VGAs in CMOS is more challenging especially due to square-law I-V characteristic of MOS transistors. Several designs have been reported in GaAs BiCMOS [7] with appropriate specs, however, CMOS is more desired owing to its low cost and low power performance [8]. Recently, some techniques have been employed in CMOS technology in order to provide logarithmic function such as using parasitic BJT [4], operating in sub-threshold region [8-9] and Taylor series approximation [10]. Each method has its own pros and cons, with possibility to trade them off to achieve an optimum architecture. In this paper, a low-power and wideband variable gain amplifier is introduced, which dB-linear characteristic is attained using MOS transistors operating in subthreshold region. In addition, the bandwidth is extended using negative capacitance in each stage and active feedback in the cascaded multi-stage VGA.

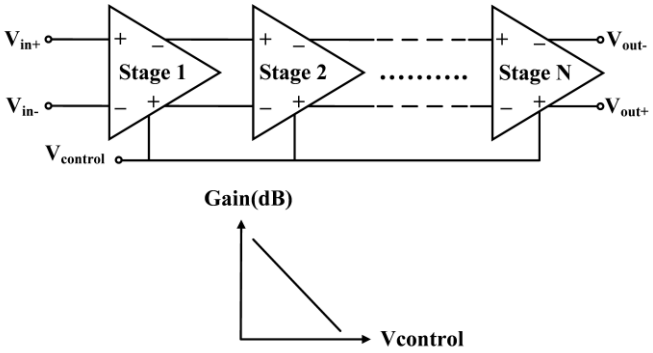

Fig. 1. N-stage cascaded VGA structure and concept of maintaining dB-linear characteristic.

II. WIDEBAND AMPLIFIER BASED ON MULTI STAGE DESIGN

Total parasitic capacitance in each node of amplifier circuits is responsible for a limited bandwidth. Additionally, because of nearly constant gain-bandwidth product (GBW) characteristic of amplifiers, higher bandwidth is usually obtained at the cost of achieving lower gain. As shown in Fig. 1, for enhancing the gain and bandwidth simultaneously, multi stage amplifiers in cascaded form is the most promising solution [11]. If the gain and bandwidth of each single-stage amplifier (cell) are identified as A_C and BW_C, respectively, it can be proved that for n cascaded stages, total gain and bandwidth are represented by [11]:

$$A_{total} = A_1 A_2 A_3 \ldots A_N \tag{1}$$

$$BW_{total} = BW_C \sqrt[m]{2^{1/N} - 1} \tag{2}$$

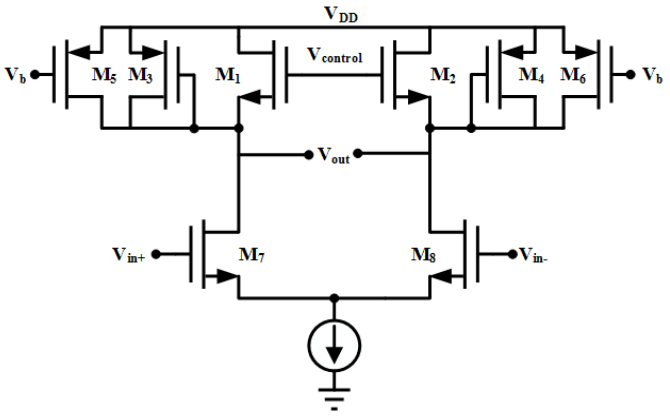

Fig. 2. VGA cell with dB-linear characteristic

where for a first order cell *m* is chosen to be 2 and 4 for the second order ones. So, with increasing the number of stages the gain is enhanced while the bandwidth degrades. For compensating this bandwidth reduction several methods are employed depending on required bandwidth [11-12], [13]. All of these approaches intend cancelling the output dominant pole by using circuits and components with inductive behavior. According to Fig. 1, it is noteworthy to say that in cascaded VGAs, each cell must have dB-linear gain control characteristic, so the overall amplifier also achieves this feature.

III. Unit Cell of the Proposed VGA

Fig. 2 shows a VGA cell with differential structure using diode connected PMOS transistors as an active load [9]. The PMOS current sources (M5, M6) are added to decrease bias current of diode connected transistors. Thus, the g_m of M3 and M4 reduces and thus a higher gain can be achieved. The NMOS transistors (M1 and M2) are biased in the sub-threshold region to obtain dB-linear characteristic while others are in saturation. In sub-threshold region, the current and voltage relationship is represented as:

$$I_D = I_{D0}\frac{W}{L}e^{V_{GS}/nV_T} \tag{3}$$

where n is the slope factor. So, the transconductances of the main transistors can be written as

$$g_{m1,2} = \frac{I_{D1,2}}{nV_T} \tag{4}$$

$$g_{m3,4,7,8} = \sqrt{2\mu_p C_{ox}\frac{W}{L}I_{D3,4}} \tag{5}$$

In Fig. 2, neglecting the body effect, the gain is derived as

$$A_V = -g_{m7,8}(g_{m1,2}^{-1} \parallel g_{m3,4}^{-1} \parallel r_{o3,4} \parallel r_{o5,6} \parallel r_{o7,8}) \tag{6}$$

By substituting (4) and (5) in (6), A_V can be rewritten as

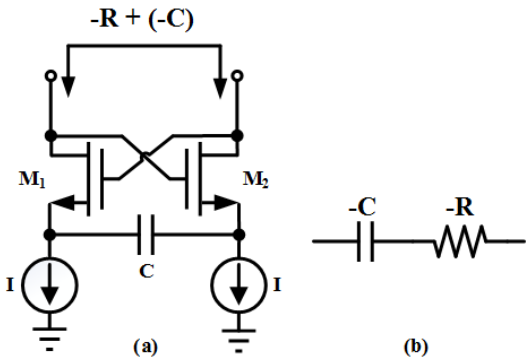

Fig. 3. Schematic of (a) a negative capacitance and (b) the equivalent circuit.

$$\begin{aligned} A_V &\approx -\frac{g_{m7,8}}{g_{m1,2}+g_{m3,4}} \\ &\approx -\frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}I_{D3,4}}}{\frac{I_{D0}}{nV_T}(\frac{W}{L})_{1,2}e^{V_{GS1,2}/nV_T}+\sqrt{2\mu_p C_{ox}\frac{W}{L}I_{D3,4}}} \end{aligned} \tag{7}$$

According to (7), the gain of the cell is proportional to $V_{GS1,2}$ exponentially. As a result, by adjusting $V_{GS1,2}$ the gain in dB varies almost linearly. So, the control voltage is applied to the gates of sub-threshold transistors (M1 and M2), to obtain a dB-linear gain range [9].

As depicted in Fig. 3(a), two cross coupled MOS transistors is the basis to produce a negative impedance. Shown in Fig. 3(b), the capacitance C is converted to a negative one in series with a negative resistance [11]. The impedance seen from the drain terminals of M1 and M2, assuming both of them are in saturation, is represented as:

$$Zin = -\frac{1}{Cs}\frac{g_m + s(C_{gs}+2C)}{g_m - sC_{gs}} \tag{8}$$

where assuming $\omega << \omega_T$, the resulted negative capacitance is –C while the amount of the series resistance is given by:

$$R = -\frac{(\frac{C_{gs}}{C}+2)}{g_m} \tag{9}$$

In order to extend the –3dB bandwidth of the VGA cell, the negative capacitance circuit is integrated with its output nodes as illustrated in Fig. 4. Since the dominant pole of the cell is associated with its output nodes, the negative capacitance (NC) circuit can help provide higher GBW.

Further bandwidth extension can be achieved using active feedback in the amplifier chain. Fig. 5 conceptually shows two cascaded amplifier with an active device as negative feedback.

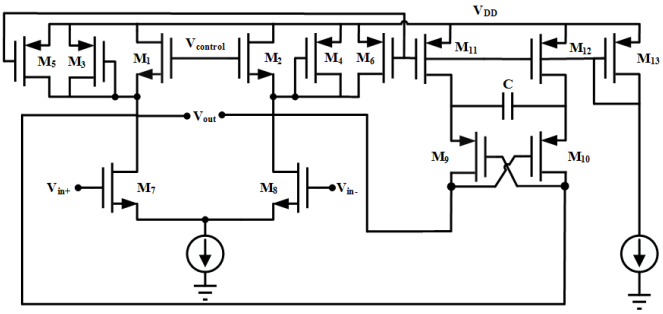

Fig. 4. Unit stage of the proposed VGA using folded negative capacitance circuit.

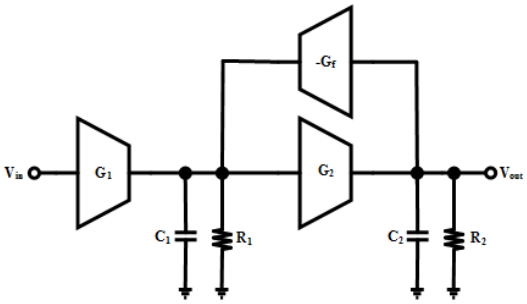

Fig. 5. The structure of the active feedback circuit.

Each G can be a differential pair [11]. The transfer function according to Fig. 5 is as follow [14]:

$$\frac{V_{out}}{V_{in}} = \frac{A_V}{\alpha_1 S^2 + \alpha_2 S + 1} \tag{10}$$

where considering R_1=R_2=R and C_1=C_2=C, we can write:

$$A_V = \frac{(GR)^2}{1+G_f GR^2} \tag{11}$$

$$\alpha_1 = \frac{(RC)^2}{1+G_f GR^2} \tag{12}$$

$$\alpha_2 = \frac{2RC}{1+G_f GR^2} \tag{13}$$

The resulted bandwidth is approximately given by

$$\omega_{-3dB} = \sqrt{\frac{1+G_f GR^2}{(RC)^2}} \tag{14}$$

Note that the bandwidth without negative active feedback was approximately

$$\omega_{-3dB} = \frac{1}{RC} \tag{15}$$

A comparison between (14) and (15) indicates that with employing active feedback, the bandwidth is extended with a factor of $\sqrt{1+G_f GR^2}$. Thus, this technique is used for enhancing the overall bandwidth of the proposed cascaded VGA.

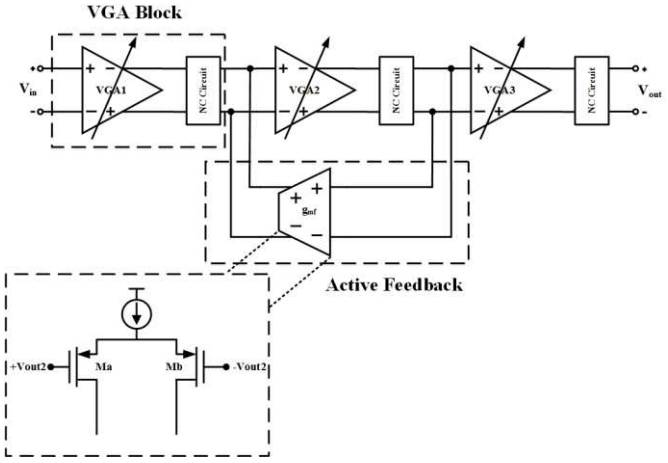

Fig. 6. Proposed cascaded VGA using active feedback.

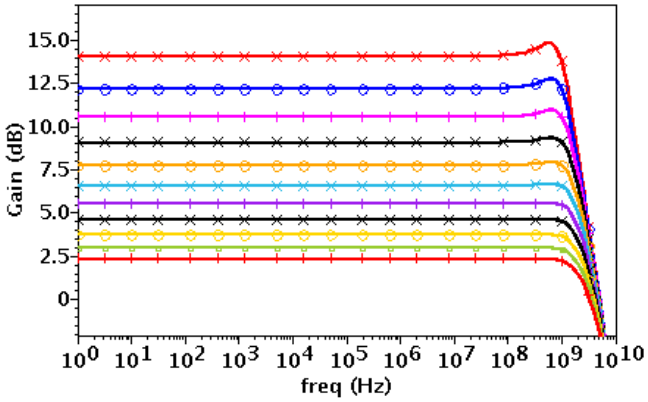

Fig. 7. Frequency response of the VGA cell combined with NC circuit in various control voltage (1.25V ~ 1.75V).

Fig. 6 shows the schematic diagram of the proposed variable gain amplifier, which includes three stages of the proposed VGA cell. An active feedback is employed over the second stage to achieve an overall broader bandwidth.

IV. Simulation Results

The proposed variable gain amplifier is simulated in a 0.18 µm CMOS technology. It consumes about 393 µA at V_{DD}=1.8 V. Fig. 7 plots the simulated frequency response of the VGA cell. When the control voltage is chosen from 1.25 V up to 1.75 V, the gain varies from 14.04 dB to 2.4 dB, respectively, while the bandwidth will also be affected. In other words, a minimum −3dB bandwidth of ~1.47 GHz is available at highest gain while the maximum −3dB bandwidth is achieved at the lowest gain at ~3.91 GHz. The value of the capacitance C in NC circuit must guarantee the minimum ringing in time domain response or accordingly peaking in frequency domain response [11]. Here, C is chosen to be 14 fF. Fig. 8 shows the frequency response of the single stage cell with and without NC circuit. Simulation

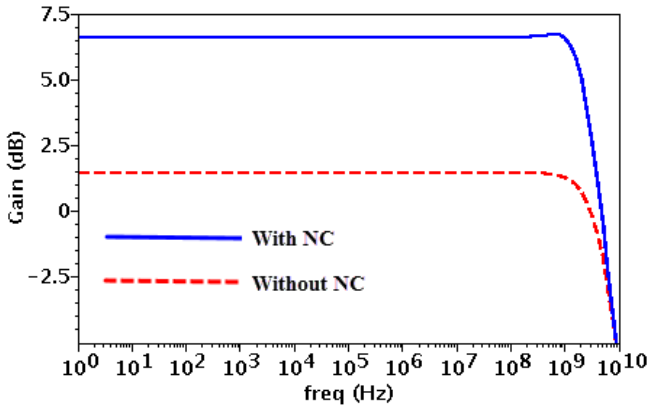

Fig. 8. Frequency response of the propose VGA cell at control voltage of 1.5 V with and without NC circuit.

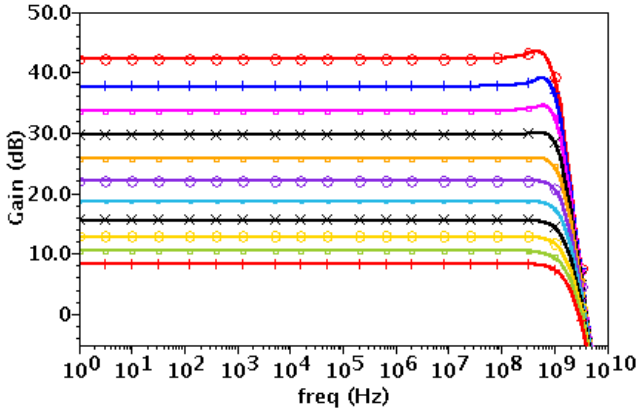

Fig. 9. Frequency response of the proposed multi-stage VGA for various control voltage (1.25V ~ 1.75V)

results indicate that with addition of the negative capacitance structure, GBW is improved about 14%.

In Fig. 9, frequency response of the three-stage VGA comprising active feedback, for a control voltage ranging from 1.25 V to 1.75 V is shown. According to this figure, the overall gain varies from 42.3 dB down to 8.4 dB, respectively, indicating about 34 dB variable gain range. Fig. 10 reveals the frequency response of the proposed VGA at a control voltage of 1.5 V, before and after employing active feedback. In a multi-stage amplifier, GBW is defined as

$$GBW_{total} = (A_C)^n . BW_C \sqrt[n]{\sqrt[N]{2}-1} \qquad (16)$$

where A_C and BW_C are the gain and bandwidth of the single stage cell, respectively. At $V_{Control}$=1.5 V, A_C and BW_C are 6.6 dB and 2.68 GHz, respectively. According to (16), after cascading three stages, the overall gain in dB should be three times larger while the bandwidths shrinks about 51%. Before utilizing active feedback, the overall gain of three stages is 19.74 dB and the bandwidth is 1.18 GHz, which conforms to (16) identifying a GBW=11.45 GHz. As shown in Fig. 10, by employing active feedback, the gain and bandwidth are 22.1 dB and 1.27 GHz, indicating a GBW of 16.17. Thus, the efficiency

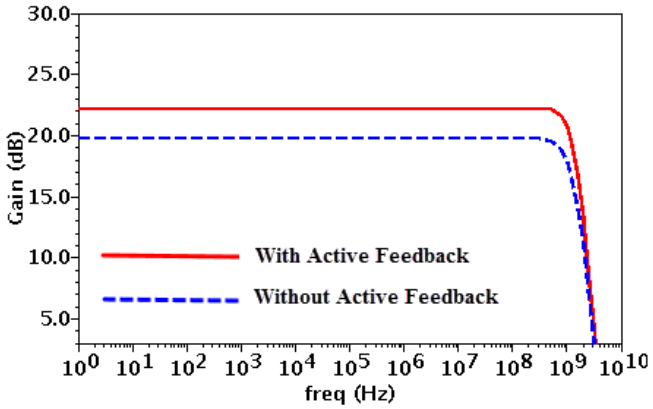

Fig. 10. Frequency response of the proposed VGA at control voltage of 1.5 V with and without active feedback.

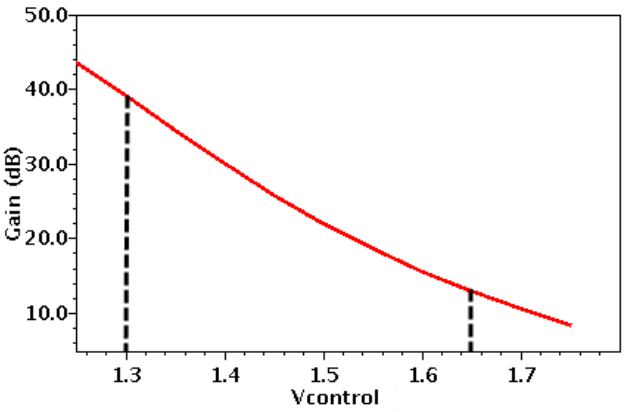

Fig. 11. Variation of gain versus control voltage in the proposed VGA.

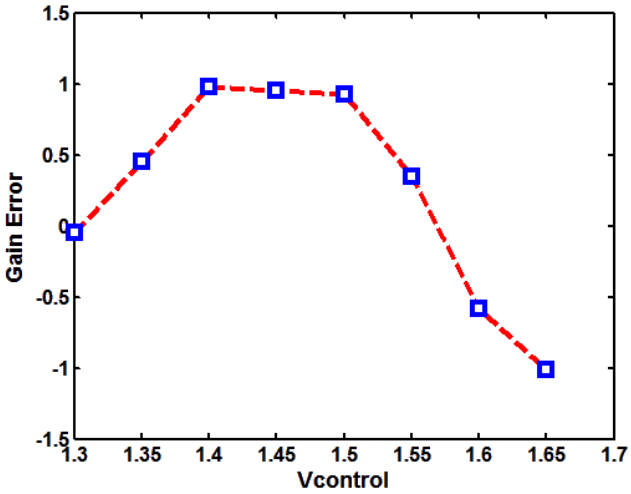

Fig. 12. Gain error versus the control voltage.

of the proposed VGA is highly clarified since the GBW has extended about 41.2%.

Table I. Performance summary and comparison with prior work

References	[8]	[9]	[14]	This work
Technology (nm)	65	180	90	180
Gain Rang (dB)	22	71	60	34
dB linear Gain (dB)	0.3	45	NA	24.8
Gain Error (dB)	0.3	1	NA	±1
BW (GHz)	2~2.2	0.05	2.2	1.1
Power (mW)	3.48	0.15	2.5	0.7

Fig. 11 depicts the simulated gain in dB versus the control voltage of the proposed VGA representing a dB linear gain range with approximately ±1 dB gain error when the control voltage varies from 1.3V to 1.65V. In this range, the gain and bandwidth start from 37.7 dB and 1.1 GHz then end by 12.9 dB and 1.5 GHz, respectively. The dependency of the gain error on the control voltage is shown in Fig. 12. The maximum gain error is about 1 dB at $V_{Control}$=1.4 V. Table I summarizes the performance of the proposed VGA and compares it with recently published work.

V. CONCLUSION

In this paper a low power and wideband variable gain amplifier with analog control voltage in 180nm CMOS technology has been introduced. The design has three sub-circuit of amplifier and includes an active feedback. Each gain stage comprises a combination of differential pair with sub-threshold load and negative capacitance circuit. Simulation results show a dB linear gain characteristic for a control voltage variation from 1.3 V to 1.65 V. A gain control range of 24.8 dB is obtained where the −3dB bandwidth is 1.1 GHz at maximum gain and 1.5 GHz for the minimum gain. At V_{DD}=1.8V, this architecture consumes only 393uA.

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