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TRIPLE-TUNNEL JUNCTION SINGLE ELECTRON TRANSISTOR (TTJ-SET)

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We propose a triple-tunnel junction single electron transistor (TTJ-SET). The proposed structure consists of a metallic quantum-dot island that is capacitive coupled to a gate contact and surrounded by three tunnel junctions. To the best of our knowledge, this is the first instance of introducing this new structure that is suitable for both digital and analog applications. I–V_{D} characteristics of the proposed TTJ-SET, simulated by a HSPICE macro model for various gate voltages, are in excellent agreement with those obtained by SIMON, which is a Monte-Carlo based simulator. We show how one can design a digital inverter by using a single TTJ-SET. We also show that, under suitable conditions, a TTJ-SET can operate as a full- or half-wave analog rectifier.

Keywords: Single electron transistor (SET); triple-junction single electron transistor (TTJ-SET), digital inverter; analog rectifier.

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1. Introduction

In recent years, nano-scale devices such as nanowires,[1] carbon nanotube field effect transistors (CNTFETs)[2,3] and single-electron transistors (SETs)[4] have attracted the device designers' attention. Operation of a SET is mainly controlled by single-electron tunneling. Its low power dissipation has made it a potential alternative for low power circuit applications.[5] During the past decade, many applications based on single-electron tunneling have been proposed. Among those are single-electron turnstile,[6] negative differential resistance (NDR) due to single-electron switching,[7] current standard and measurement,[8] smart universal multiple-valued logic gates,[9] voltage controlled ring oscillators,[10] neural cells,[11] CMOS-like logic gates,[12–14] non-CMOS-like logic gates[15,16] and CMOS-like digital inverters.[17–19]

A conventional SET consists of a quantum-dot (QD) island placed between two tunnel-junctions, similar to a channel sandwiched between source (S) and drain (D) in a conventional FET structure. In this paper, by adding one more tunnel-junction to the metallic QD-island of a conventional SET, we have proposed a new triple-tunnel junction SET (TTJ-SET) whose schematic representation is illustrated in Fig. 1. A remarkable advantage of the proposed structure is that a single TTJ-SET solely is enough for designing a digital inverter. Whereas, for implementing similar inverter based on conventional SETs at least two Transistors are required.[17–19] Furthermore, a TTJ-SET has the capability of operating as a full- or half-wave rectifier in analog applications.

The rest of this paper is organized as follows. In Sec. 2, a qualitative description of the operating principles of the proposed TTJ-SET, under various biasing conditions, is presented. In Sec. 3, we present the device modeling which covers the governing equations as well as the equivalent circuit model. In Sec. 4, we illustrate the simulation results accompanied with discussions. This paper, is finally, concluded in Sec. 5.

2. Operating Principles

In most circuit applications, the two tunnel-junctions (S) and (D) are distinguished by junction capacitances (C_S and C_D) and tunneling resistances (R_S and R_D). Realization of SETs by resistive coupling of the tunnel-junctions to the QD island (R-SET) is also possible. Nevertheless, resistive coupling leads to the Nyquist noise issue.[20] In a conventional capacitive coupled SET, the current flowing from D to S is controlled by an external voltage applied to a gate (G) that is capacitively coupled to the QD-island, and the currents flowing into the drain (I_D) and out from the source ($-I_S$) are equal.

As illustrated in Fig. 1, the third tunneling junction in the proposed TTJ-SET is designated by J_3, with junction capacitance and tunneling resistance of C_{J3} and R_{J3}. The current flowing into this terminal is labeled I_{J3}. The external voltages applied to the device terminals are labeled V_G, V_D, V_S, and V_{J3}, accordingly.

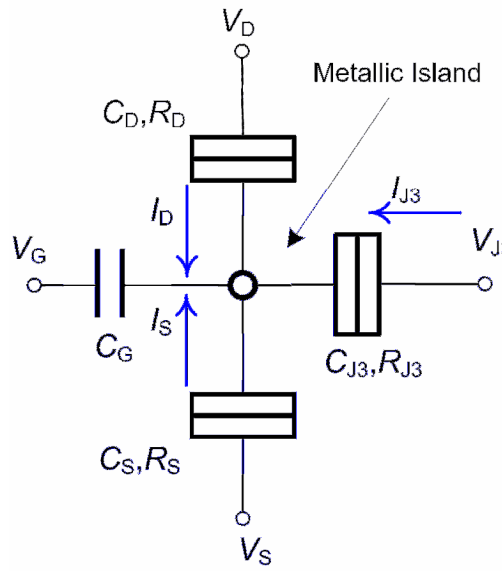


Fig. 1. A schematic representation of the proposed TTJ-SET model.

To explain the device operation we consider five cases, which depend on the biasing conditions and the tunneling resistances and capacitances.

Case 1: $R_S = R_D$, $C_S = C_D$, $V_D = -V_S$, $V_{J3} = 0$, and $V_G = 0$. In this case, the island charging energy level is almost zero, and hence, $I_{J3} = 0$. Furthermore, as long as V_{DS} is kept below the Coulomb blockade threshold, no current flows across the island (i.e. $I_D = -I_S = I_{J3} = 0$). As V_{DS} is increased beyond the Coulomb blockade threshold, the current only flows between the drain and the source ($I_D = -I_S > 0$ and $I_{J3} = 0$). Note that C_{J3} and R_{J3} may or may not be equal to their counterparts $R_{S,D}$ and $C_{S,D}$.

Case 2: $R_S = R_D$, $C_S = C_D$, $V_D = -V_S$, $V_{J3} = 0$, and $V_G > 0$. In this case, the island charging energy level moves away from the source Fermi level (E_{FS}) and approaches that of the drain (E_{FD}). Hence, for V_{DS} beyond the Coulomb blockade $I_D < -I_S$ and $I_{J3} > 0$. That is, the tunneling between the island and the source is stronger than that between the drain and the island and I_{J3} flows from J_3 into the island.

Case 3: $R_S = R_D$, $C_S = C_D$, $V_D = -V_S$, $V_{J3} = 0$, and $V_G < 0$. In this case, the island charging energy level moves away from E_{FD} and approaches E_{FS} — i.e., opposite to the direction in Case 2. Hence, for V_{DS} beyond the Coulomb blockade $-I_S < I_D$ and $I_{J3} < 0$. That is, the tunneling between the island and the source is weaker than that between the drain and island and I_{J3} flows from the island into J_3.

Case 4: $R_S = R_D$, $C_S = C_D$, $|V_D| \neq |V_S|$, and $V_{J3} = 0$. In this case, the asymmetry in the source and the drain biases forces the island charging energy

level to deviate from zero, even for $V_G = 0$. Hence, under any appropriate biasing condition that can overcome the Coulomb blockade, currents can tunnel through all three junctions, and I_D, I_S, and $I_{J3} \neq 0$.

Case 5: $R_S \neq R_D$, $C_S \neq C_D$, $V_D = -V_S$, and $V_{J3} = 0$. In this case, the asymmetry in source and drain junctions forces the island charging energy level to deviate from zero, even for $V_G = 0$ (similar to that in Case 4). Hence, for V_{DS} beyond the Coulomb blockade, currents can tunnel through all three junctions, and I_D, I_S, and $I_{J3} \neq 0$.

3. Modeling

3.1. *Governing equations*

The tunneling rate across any tunnel junctions that is formed between a metallic island and a metallic (S/D) contact can be calculated based on Orthodox theory. In this paper, as we have discussed in Sec. 2, the tunnel junctions are modeled with their corresponding resistances and capacitances, and the gate contact is represent by its capacitance C_G. According to the Orthodox theory, the rate of tunneling from any tunnel-junction, j (i.e., D, S, or J_3), into an island, i, containing n electrons can be written as[20]

$$\Gamma_{n\to n+1}^{j\to i} = \frac{1}{e^2 R_j} \frac{\Delta F_{n\to n+1}^{j\to i}}{\exp(\Delta F_{n\to n+1}^{j\to i}/k_B T) - 1}, \tag{1}$$

where k_B, T, and e are the Boltzmann constant, temperature, and the electronic charge, respectively. $F_{n\to n+1}^{j\to i}$ is the Helmholtz free energy, which is the difference between the internal (electrostatic) energy of the system and the work done on the system provided by the voltage and the current sources,

$$\Delta F_{n\to n+1}^{j\to i} = (E_{ch}(n+1) - E_{ch}(n)) - (-eV_j) \tag{2}$$

represents the change in the Helmholtz free energy that is equivalent to the useful energy available in the system, which in turn, equals the difference between the free energies available in the system before and after each tunneling event that adds an electron to the island,

$$E_{ch}(n) = \frac{(-en + Q_{ext})^2}{2C_\Sigma} \tag{3}$$

is the electrostatic energy of an island containing n electrons that is influenced by the external charges, $Q_{ext} = C_G V_G + C_S V_S + C_D V_D + C_{J3} V_{J3}$, and $C_\Sigma = C_G + C_S + C_D + C_{J3}$ is the total capacitance.

According to the Eq. (2), when a single electron is added to an island, the change in the Helmholtz free energy becomes negative. The total tunneling rate into the island equals the sum of the tunneling rates from individual contacts into the island,

$$\Gamma_{n\to n+1} = \sum_j \Gamma_{n\to n+1}^{j\to i}. \tag{4a}$$

Similarly, when an electron tunnels out of an island populated by n electrons, the total rate of tunneling out of the island may be written as

$$\Gamma_{n\to n-1} = \sum_j \Gamma^{j\to i}_{n\to n-1}\,. \tag{4b}$$

Knowing the tunneling rates and the probability of n electrons being in the island (p_n) that can be determined by the master equations,[4] the total current that tunnels through the contact j can be written as:

$$I_j = -e\sum_j p_n(\Gamma^{j\to i}_{n\to n+1} - \Gamma^{j\to i}_{n\to n-1})\,. \tag{5}$$

Equations (1) to (5) can be used to model of the proposed TTJ-SET with HSPICE.

3.2. *Circuit model*

SPICE macro model simulator has been used to model conventional SETs.[5,18,22,23] In reality, some of SET's inherent characteristics, such as Coulomb oscillation that is randomly disturbed by thermal fluctuations and co-tunneling, cannot be simulated by SPICE macro model. However, it has been shown that when operating temperature is $T \ll e^2/2C_\Sigma k_\mathrm{B}$ and $V_\mathrm{DS} > e/C_\Sigma$ (i.e. drain to source voltage overcomes the Coulomb blockade threshold), the compact macro model of SPICE can well describe the SET's behavior.[10] On the other hand, SPICE macro model may be used to simulate circuits consisting more than one SET under a specific condition. That is, only if the capacitance of each node, interconnecting the adjacent SETs, is large enough for each SET to be regarded as an independent element. In that case, characteristic of each SET solely depends on the voltages applied to the nodes that connect it to the adjacent SETs.[24]

Using a similar method as used by Zhang *et al.*,[5] for SET-based nano-circuit simulation, we have used HSPICE to simulate the proposed TTJ-SET. This technique, in which a conventional SET is modeled by a voltage-controlled current-source, is based on the steady state master equation. Calculation of the device current is based on the Orthodox theory and the Birth–Death Markov chain. As we have discussed in Sec. 2, for Cases 2–5, currents tunneling through S, D, and J_3 ($I_\mathrm{S}, I_\mathrm{D}$, and I_{J3}) differ from each other. Hence, for the HSPICE macro model that we have developed to simulate the proposed TTJ-SET, we use three voltage-controlled current-sources (G_1, G_2, and G_3), as illustrated in Fig. 2. As shown in this figure, $G_1 \equiv f(V_\mathrm{G}, V_\mathrm{D}, V_\mathrm{S}, V_{J3})$, $G_2 \equiv g(V_\mathrm{G}, V_\mathrm{D}, V_\mathrm{S}, V_{J3})$, and $G_3 \equiv h(V_\mathrm{G}, V_\mathrm{D}, V_\mathrm{S}, V_{J3})$ correspond to S, D, and J_3, respectively. These three current-sources are given by

$$G_1 = -e\sum_n p_n(\Gamma^{D}_{n\to n+1} - \Gamma^{D}_{n\to n-1})\,. \tag{6}$$

$$G_2 = -e\sum_n p_n(\Gamma^{S}_{n\to n+1} - \Gamma^{S}_{n\to n-1})\,. \tag{7}$$

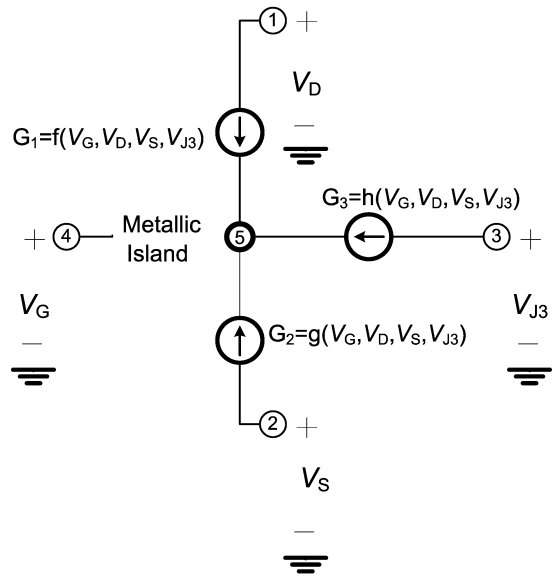


Fig. 2. HSPICE macro model of TTJ-SET.

$$G_3 = -e \sum_n p_n (\Gamma^{J3}_{n \to n+1} - \Gamma^{J3}_{n \to n-1}) \,. \tag{8}$$

4. Simulation Results

In order to illustrate the validity of the proposed TTJ-SET macro model, we have compared I–V characteristics obtained by HSPICE and those obtained by SIMON.[25] The latter simulator that is based on Monte Carlo method has been extensively used to study circuits based on SETs with metallic QD-islands. In both simulations, we have assumed the temperature to be $T = 4.2$ K. The total capacitance that must satisfy $C_\Sigma \ll e^2/2k_B T$,[10] at this temperature, is far less than 228.5 aF. In our simulations, we have assumed $C_\Sigma \leq 5$ aF that satisfies the aforementioned condition and is comparable to those used by Refs. 9, 10, 13 and 17. In these calculations, we have taken eleven charging states into account (i.e. $n-5$ to $n+5$), which limits the model validity to the bias voltages in the range of -160 mV $= -5e/C_\Sigma < V_D < +5e/C_\Sigma = +160$ mV.

Figures 3 and 4 show $I_D - V_D$ and $I_{J3} - V_D$ characteristics for a TTJ-SET with $R_D = R_S = R_{J3} = 1$ MΩ, $C_D = C_S = C_{J3} = 1$ aF and $C_G = 1.5$ aF, biased at $V_S = -V_D$, $V_{J3} = 0$, and $V_G = 0$ (solid line), 20 (dashed-line), and 40 mV (dots), obtained by HSPICE. Open circles denote the results obtained by SIMON. The comparison demonstrates that there is an excellent agreement between the results obtained by HSPICE and SIMON simulators.

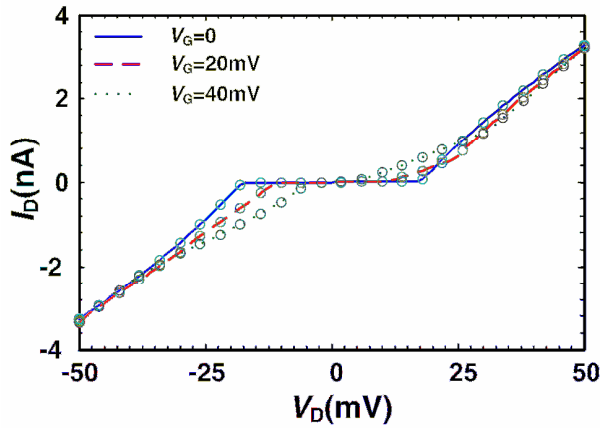


Fig. 3. $I_D - V_D$ characteristics of TTJ-SET with $R_D = R_S = R_{J3} = 1$ MΩ, $C_D = C_S = C_{J3} = 1$ aF and $C_G = 1.5$ aF for $V_G = 0$, 20 mV, 40 mV, $V_S = -V_D$, and $V_{J3} = 0$. Dots, dashed-line and solid-line denote the results obtained by HSPICE, and circles illustrate those obtained by SIMON.

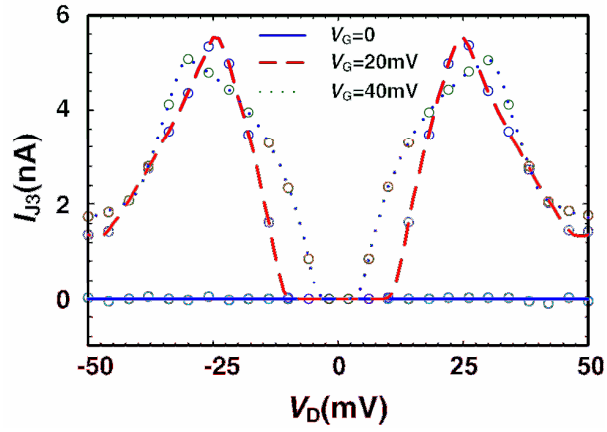


Fig. 4. $I_{J3} - V_D$ characteristics for TTJ-SET with $R_D = R_S = R_{J3} = 1$ MΩ, $C_D = C_S = C_{J3} = 1$ aF, and $C_G = 1.5$ aF for $V_G = 0$, 20 mV, 40 mV, $V_S = -V_D$, and $V_{J3} = 0$. Dots, and dashed and solid lines denote results obtained by HSPICE, and circles illustrate results obtained by SIMON, for the sake of comparison.

As pointed out earlier, for the case shown in Fig. 3, $V_{J3} = 0$. Hence, as shown in this figure, when $V_G = 0$ and V_D is relatively small ($|V_D| < 17.5$ mV), Coulomb blockade is the dominant mechanism. However, by increasing V_G, one can overcome the blockade with smaller drain voltages (i.e. $V_D < 10$ and 4 mV for $V_G = 20$ and 40 mV, respectively).

On the other hand, as shown in Fig. 4 for $V_G = 0$, $I_{J3} = 0$ for all drain voltages (Case 1 in Sec. 2). For $V_G > 0$ and $V_D > 0$ the difference between the drain Fermi

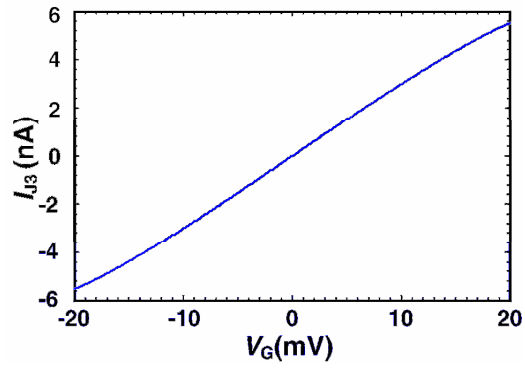


Fig. 5. $I_{J3} - V_G$ characteristic of TTJ-SET with $R_D = R_S = R_{J3} = 1$ MΩ, $C_D = C_S = C_{J3} = 1$ aF, and $C_G = 1.5$ aF, acting as an inverter biased at $V_D = -V_S = 25$ mV and $V_{J3} = 0$.

level and the island charging level is less than the difference between the island charging level and the source Fermi level. Hence, when V_D is increased beyond the coulomb blockade threshold, I_{J3} is positive (Case 2 in Sec. 2). As also seen in Fig. 4, $I_{J3} - V_D$ characteristic is symmetric because for $V_D < 0$ the role of S and D contacts are altered.

In a CMOS-like inverter based on SET, the *p*- and *n*-MOS transistors are replaced by two equivalent SETs. Hence, such an inverter consists of four tunneling junctions, and two gates with two coupled capacitors. Instead, by using a single TTJ-SET including three tunnel junctions and one gate-coupled capacitor one can implement a digital inverter with a similar capability. Before demonstrating this possibility, by illustrating the simulated $I_{J3} - V_G$ characteristic of the model presented in Fig. 1 with $R_D = R_S = R_{J3} = 1$ MΩ, $C_D = C_S = C_{J3} = 1$ aF and $C_G = 1.5$ aF biased at $V_D = -V_S = 25$ mV and $V_{J3} = 0$, we demonstrate the inverting behavior of the proposed TTJ-SET. The $I_{J3} - V_G$ characteristic that is illustrated in Fig. 5 follows the Case 2 for $V_G > 0$ with $I_{J3} > 0$ and Case 3 for $V_G < 0$ with $I_{J3} < 0$.

Now, by connecting the terminal J_3 to the ground via a resistance (R), we propose a model for the TTJ-SET based digital inverter. As illustrated in Fig. 6, this new proposed digital inverter is, indeed, simpler and smaller than a conventional SET based inverter.

By assuming appropriate values for resistances and capacitances (e.g. $R_S = R_D = 1$ MΩ, $R_{J3} = 0.1$ MΩ, $C_D = C_S = 0.65$ aF, $C_{J3} = 0.1$ aF, $C_G = 2.7C_D$, and $R = 10$ MΩ) an adequate level of output voltage, for the inverter of Fig. 6, can be achieved. Figure 7 illustrates the inverter transfer characteristic ($V_{OUT} - V_{IN}$) obtained for $V_D = -V_S = 25$ mV and a quasi-statically varying input level ($0 < |V_{IN}| < 20$ mV).

The inverting behavior with a low noise margin seen in this figure is a consequence of symmetries in S and D junctions and their biases. This transfer

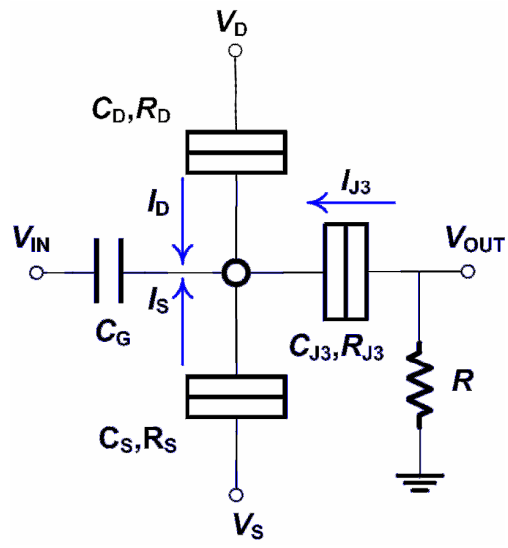


Fig. 6. Circuit model for a TTJ-SET based inverter.

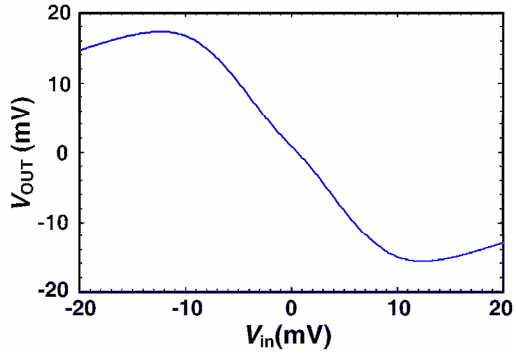


Fig. 7. Transfer characteristic of the TTJ-SET based inverter of Fig. 6 with $R_D = R_S = R_{J3} =$ 1 MΩ, $C_D = C_S = 0.65$ aF, $C_G = 2.7C_D$, $C_{J3} = 0.1$ aF and $R = 10$ MΩ for $V_D = -V_S = 25$ mV.

characteristic shows that appropriate input signal levels are −15 mV and +15 mV that correspond to logic levels zero and one, respectively. Now, we apply signals with square waveforms of the same levels (±15 mV) but various frequencies, as illustrated in Fig. 8(a), to the input of the circuit shown in Fig. 6. Note that the time scale for each input signal (i.e. the horizontal axis) is normalized with respect to the signal's period. By varying the signals' frequencies from $f = 1$ to 100 GHz, we have realized that as it approaches 10 GHz the inverter output levels response experiences some ringing oscillations and the output response becomes distorted. Figure 8(b) illustrates the output responses for $f = 1$, 10, and 100 GHz, as an

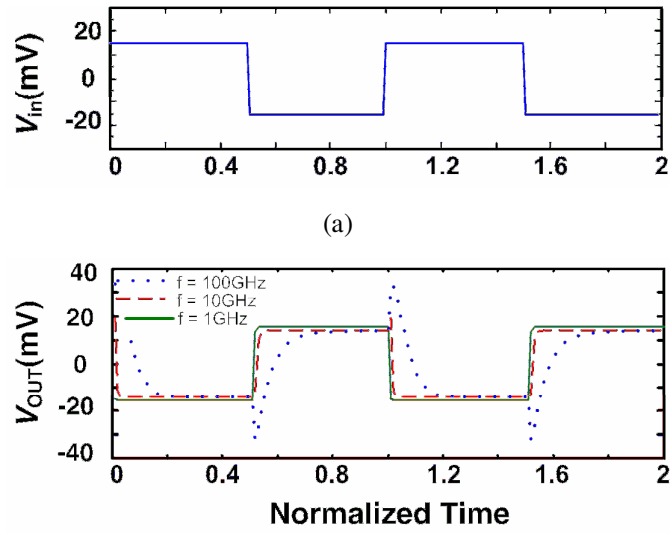
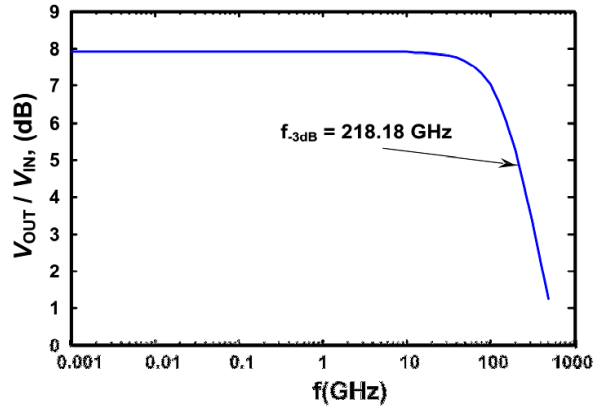


Fig. 8. (a) Time domain representation of (a) input signals of frequencies $f = 1$, 10, and 100 GHz with square waveforms of the same voltage levels (± 15 mV), applied to the inverter of Fig. 6; (b) the output response of the inverter to the input waveform shown in (a). Horizontal axis is normalized to the period of the input signal, T.

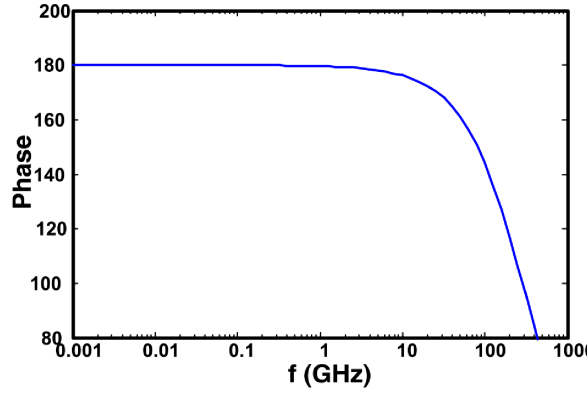
example. Horizontal axis of this figure is also normalized, as that of Fig. 8(a). As shown in Fig. 8(b), the output response for $f = 1$ GHz (solid line), in the time domain, is an inverted replica of the input signal. However, as also illustrated in this figure, the output levels for $f = 10$ GHz (dashed-line) and 100 GHz (dots) are distorted.

In order to obtain the gain and the frequency bandwidth of the inverter, we have simulated its frequency response to sinusoidal input small signals of various frequencies. Figure 9(a) illustrates the frequency response for the amplitude of the inverter output signal. This figure shows that inverter enjoys from a gain of 8 dB and a -3dB frequency bandwidth of about 218 GHz. The frequency response for the phase of the inverter output is shown in Fig. 9(b). As shown in this figure, as the frequency approaches $f = 10$ GHz, the phase starts to reduce notably, which in turn distorts the resulting output signal.

As pointed out earlier, another potential application for the proposed TTJ-SET is a full- or half-wave analog rectifier. In order to reveal this potential for the proposed TTJ-SET, at first, we consider a circuit like that shown Fig. 10. Then, we apply two out of phase signals of the same frequency (f) and amplitude (V_m) to terminals D and S (i.e. $V_{\rm D} = V_{\rm IN} = V_m \sin(2\pi f t)$ and $V_{\rm S} = -V_{\rm IN}$), and simulate the transfer characteristics for various gate voltages.



(a)



(b)

Fig. 9. Frequency response for of the output of the inverter of Fig. 6 with $R_S = R_D = 1$ MΩ, $R_{J3} = 0.1$ MΩ, $C_D = C_S = 0.65$ aF, $C_G = 2.7C_D$, $C_{J3} = 0.1$ aF and $R = 10$ MΩ for $V_D = -V_S = 25$ mV: (a) the amplitude, (b) phase.

Figure 11 illustrates the resulting transfer characteristics ($V_{OUT} - V_{IN}$), for $V_G = -5$ mV (dashed-line), -15 mV (solid line), and -30 mV (dots), as an example. This figure demonstrates the behavior of a full-wave analog rectifier. As observed in this figure, the peaks of the rectifier transfer characteristics increase, as V_G becomes more negative and shift toward higher input levels ($|V_{IN}|$). As also seen in this figure, for a given V_G, when the input level is below the Coulomb blockade threshold (i.e. $|V_{IN}| \leq 5.6$ mV for $V_G = -30$ mV, $|V_{IN}| \leq 10$ mV for $V_G = -15$ mV, and $|V_{IN}| \leq 15$ mV for $V_G = -5$ mV) there is no output level. This is because, under this condition no current can tunnel through any of the three tunnel-junctions and hence $V_{OUT} = 0$.

On the other hand, for large $|V_G|$ values, as the input level increases beyond a certain value (e.g. $|V_{IN}| > 26$ mV for $V_G = -30$ mV), the output level experiences

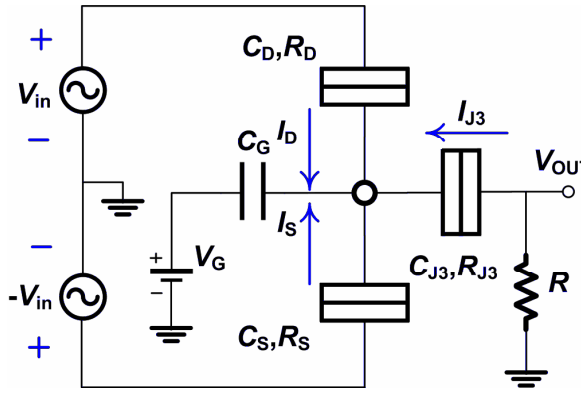


Fig. 10. Circuit model for a full-wave TTJ-SET rectifier.

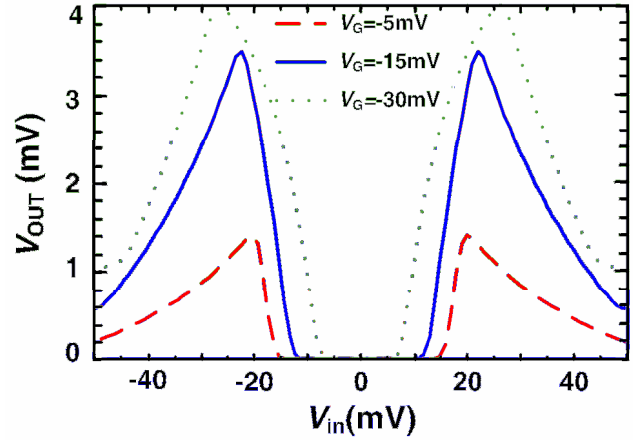


Fig. 11. Transfer characteristic of the rectifying TTJ-SET of Fig. 10, with $R_S = R_D = 1$ MΩ, $R_{J3} = 300$ kΩ, $C_D = C_S = 1$ aF, $C_G = 1.5C_D$, $C_{J3} = 1$ aF and $R = 1$ MΩ for $V_G = -5$ mV (dashed-line), -15 mV (solid line), and -30 mV (dots).

some distortion. In fact, for $V_G = -30$ mV and 5.6 mV $< |V_{IN}| <$ 26 mV, $|I_D| > |I_S|$ and $|dI_D|/d|V_{IN}| > |dI_S|/d|V_{IN}|$. Hence, $|I_{J3}|$ increases with $|V_{IN}|$, which results in a normal rectifying behavior. However, for $V_G = -30$ mV and $|V_{IN}| >$ 26 mV, although $|I_D| > |I_S|$ and $I_{J3} < 0$, $|dI_D|/d|V_{IN}| < |dI_S|/d|V_{IN}|$ and hence $|I_{J3}|$ and V_{OUT} both decrease with an increase in $|V_{IN}|$. This in turn, results in an abnormal (distorted) transfer characteristic. In order to examine such abnormalities further, consider a case in which $V_G = -30$ mV and three input signals of amplitudes $V_m = 10$, 20 and 30 mV with the same frequency ($f = 1$ MHz) as an example and simulate $V_{OUT}(t)$. Figure 12 illustrates the resulting characteristics.

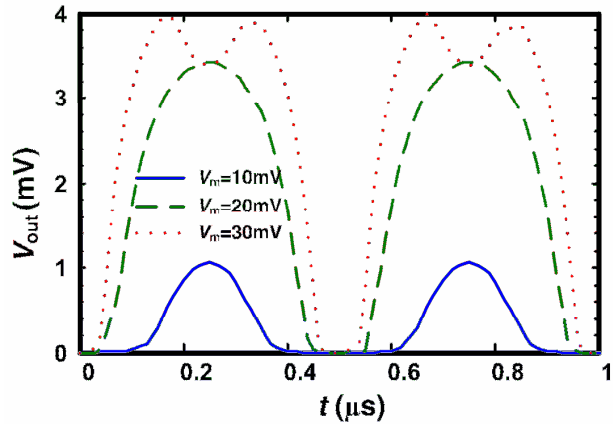


Fig. 12. Variation in $V_{\mathrm{OUT}}(t)$ of the proposed full-wave rectifier of Fig. 10, for $V_{\mathrm{G}} = -30$ mV, over one period of three input signals of the same frequency ($f = 1$ MHz) and amplitudes $V_m = 10$ (solid line), 20 (dashed line), and 30 mV (dots). $R_{\mathrm{S}} = R_{\mathrm{D}} = 1$ MΩ, $R_{J3} = 300$ kΩ, $C_{\mathrm{D}} = C_{\mathrm{S}} = 1$ aF, $C_{\mathrm{G}} = 1.5C_{\mathrm{D}}$, $C_{J3} = 1$ aF and $R = 1$ MΩ.

As observed in this figure, for $V_m = 10$ mV (solid line) and 20 mV (dashed-line) the output levels do not experience any distortion at any time. However, for the input signal with $V_m = 30$ mV (dots), during those periods of times that $|V_{\mathrm{IN}}| > 26$ mV, as illustrated in Fig. 12, $V_{\mathrm{OUT}}(t)$ decreases as $|V_{\mathrm{IN}}|$ increases and the rectifier transfer characteristic becomes distorted. In other words, the rectifier experiences some abnormalities. Obviously, for $V_{\mathrm{G}} > 0$, the resulting characteristics are the same as those illustrated in Figs. 11 and 12, except for the singe of the output levels that become negative.

In order to obtain a half-wave rectifier, one may directly ground the terminal S of the rectifier shown in Fig. 10. Variations in V_{OUT} versus time for this half-wave rectifier over two periods of the input signal, for $V_{\mathrm{G}} = -30$ mV and $V_m = 20$ mV, as an example, is illustrated in Fig. 13.

5. Conclusion

A new triple-tunnel junction single electron transistor (TTJ-SET) has been proposed. Using a SPICE macro model, we have simulated the behavior of the proposed TTJ-SET by HSPICE simulator. In a comparison, these results were shown to be in excellent agreement with those obtained by the SIMON simulator that is a Monte Carlo based software. We have also shown that a single TTJ-SET can be used to design a digital inverter with 8 dB flat-band gain and 218 GHz bandwidth. Simulations have shown that the inverter performance depends strongly on the junctions' parameters. Furthermore, we have shown that a TTJ-SET can also be used as either a full-wave or a half-wave analog rectifier, under appropriate biasing conditions.

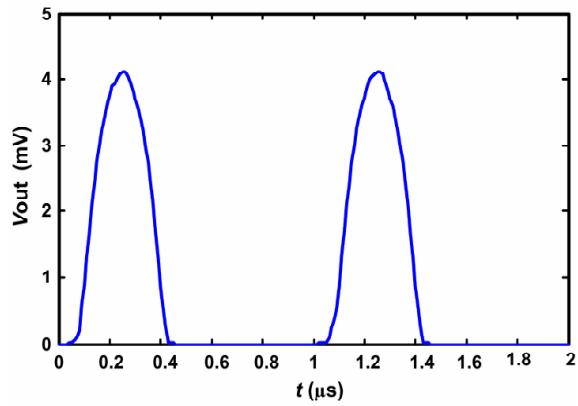


Fig. 13. Variation in $V_{\mathrm{OUT}}(t)$ of the proposed half-wave rectifier, for $V_{\mathrm{G}} = -30$ mV, over two period of an input signals of frequency $f = 1$ MHz and amplitude $V_m = 20$ mV. $R_{\mathrm{S}} = R_{\mathrm{D}} = 1$ MΩ, $R_{J3} = 300$ kΩ, $C_{\mathrm{D}} = C_{\mathrm{S}} = 1$ aF, $C_{\mathrm{G}} = 1.5C_{\mathrm{D}}$, $C_{J3} = 1$ aF and $R = 1$ MΩ.

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