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NUMERICAL INVESTIGATION ON THE TEMPERATURE DEPENDENCE OF THE CYLINDRICAL-GATE-ALL-AROUND Si-NW-FET

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We report the results of our numerical investigation on the temperature dependence of the characteristics of the cylindrical gate-all-around Si nanowire field effect transistor (Si-NW-FET). Assuming the effect of temperature on the energy band structure of Si just like the effect of strain, we simulate the transistor characteristics at various temperatures (50 K $\leq T \leq$ 300 K). In this investigation, we demonstrate the temperature dependence of the transistor sub-threshold swing and the threshold voltage are both linear functions of the temperature, represented by $61.5 \times (T/300) + 63.4$ (mV/decade) and $220–140 \times (T/300-1)$ (mV). By calculating the $I_{DS}-T$ characteristics for $V_{DS} = 0.4$ V and various V_{GS}, we show that the temperature sensitivity of the drain current defined as the slope of the $I_{DS} - T$ plot, for a given V_{GS}, is independent of the temperature and increases with V_{GS} in a quadratic manner $[-150 \times (V_{GS} - 0.50)^2 + 8.5$ (nA/K)]. Ultimately, the dependence of the transistor delay time on temperature will be presented.

Keywords: Energy band structure; Si-nanowire field effect transistor (NW-FET); temperature sensitivity.

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1. Introduction

Nanowire field effect transistors (NW-FETs), whose characteristics are dominated one-dimensional carrier transport, have attracted a great attention in recent years.[1–4] Cylindrical nanowire with gate-all-around provides full electrostatic control, and hence, leads to further device miniaturization. Many research groups have focused on the effects temperature on the NW-FETs.

Experimental studies by Cho *et al.*[1] on gate all around twin Si-NW-FET show that as temperature decreases, the sub-threshold swing and off-current also decrease. By measuring the temperature dependent of I–V characteristics for ZNO-NW-FET, Ju *et al.*[2] and Chang *et al.*,[3] independently show that a decrease in temperature lead to an increase in the threshold voltage and hence a decrease in the drain current. Similar temperature dependence for characteristics of InAs and InSb NW-FETs has also been reported by Nilsson *et al.*[4]

To the best of our knowledge, theoretical modeling of temperature dependence of Si-NW-FET characteristics has not been reported to date. Focus of this paper is on such a theoretical modeling for cylindrical gate-all-around Si-NW-FET. Having presented a model to consider the temperature dependence of the transistor characteristics, sensitivity of the drain current on the temperature in the saturation region, and its dependence on the gate voltage and thickness of the gate oxide have been also studied. Moreover, from this we have also developed an analytical expression for this sensitivity. Furthermore, a similar analytical expression has been presented for the sub-threshold region. Finally, from the latter analytical model we have studied the temperature effect on the transistor delay time.

Rest of this paper is organized as follows. In Sec. 2, following a brief overview of the device structure, the proposed theoretical model is introduced. Section 3 is dedicated to the simulation results and discussion. Finally, the paper is closed by conclusion in Sec. 4.

2. The Proposed Model and Simulation Method

Figure 1 illustrates a schematic representation of cylindrical gate-all-around Si-NW-FET, under study. The channel is made of a 10-nm long cylindrical Si nanowire of diameter $d_{ch} = 2.75$ nm, whose crystallographic orientation is [100]. It is covered by a layer of SiO_2 of thickness $d_{ox} = 1$ nm.

Numerical simulations are based on the ballistic model of Fig. 2 that was first introduced by Rahman *et al.*[5] Parameters E_{FS} and E_{FD} are the source and drain Fermi levels, respectively U_{SCF} is the coupling of electrostatic potential at the top of the barrier with the gate, drain, and source terminal that is given by:[5]

$$U_{\mathrm{SCF}} = \alpha_G V_G + \alpha_D V_D + \alpha_S V_S + \frac{Q_{\mathrm{Top}}}{C_\Sigma} \tag{1}$$

where $C_\Sigma = C_G + C_D + C_S$, with C_G, C_D and C_S, being the gate, the drain and the source capacitances, respectively, V_G, V_D and V_S are the corresponding terminal

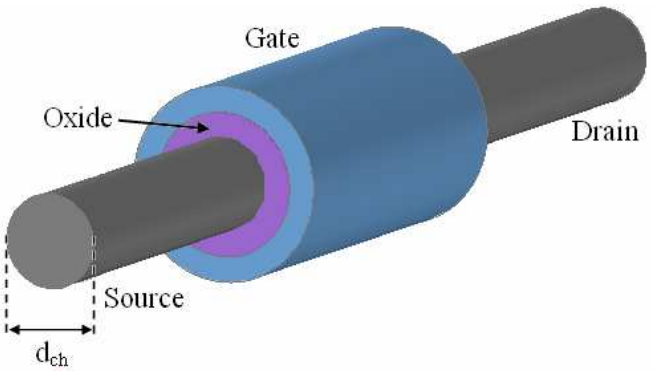

Fig. 1. Schematic representation of cylindrical Si-NW-FET. The channel length and diameter are $L = 10$ nm and $d_{ch} = 2.75$ nm, respectively, and thickness of the gate oxide is $d_{ox} = 1$ nm.

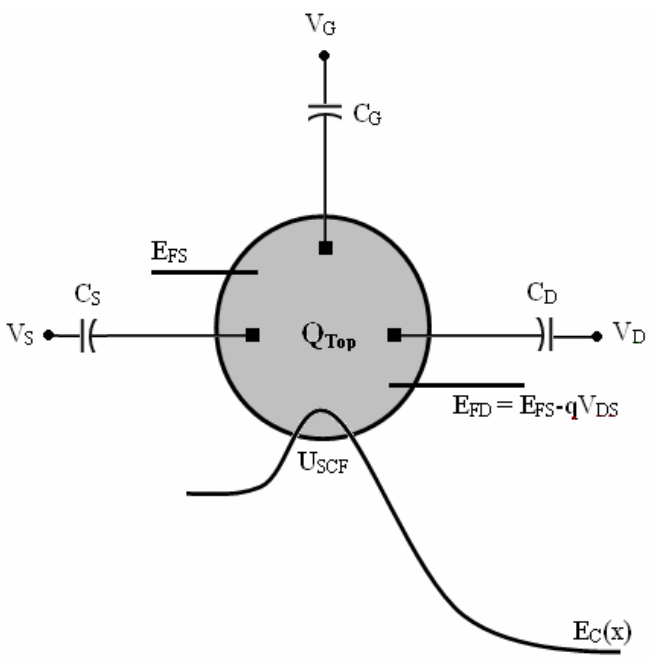

Fig. 2. Schematic diagram of the ballistic model for the Si-NW-FET of Fig. 1.

voltages, $\alpha_G = C_G/C_\Sigma$, $\alpha_D = C_D/C_\Sigma$ and $\alpha_S = C_S/C_\Sigma$ and $Q_{\rm Top}$ is the mobile charge at the top of the barrier which in turn is determined by $U_{\rm SCF}$:

$$Q_{\rm Top} = -\frac{q}{2\ell}[\Im_{-\frac{1}{2}}(\eta) + \Im_{-\frac{1}{2}}(\eta - U_D)]\,, \tag{2}$$

where $\eta = \{E_{FS} - [\varepsilon(0) - qU_{\rm SCF}]\}/k_BT$, $\ell = M^{-1}(\pi\hbar^2/2k_BTm_x^*)^{1/2}$, q is the electron charge, $\hbar$ is the reduced Planck constant, k_B is the Boltzmann constant,

T is the ambient temperature, M is the valley degeneracy, $m_x^* = m_t m_0$ in which m_t is the electron effective mass in the transport direction and m_0 is electron rest mass in free space, $U_D = qV_{DS}/k_BT$, $\varepsilon(0)$ is the least subband level at the top of the barrier when $U_{\mathrm{SCF}} = 0$, and

$$\Im_{-\frac{1}{2}}(\eta) = \Gamma(1/2)^{-1}(1 + \exp(1 - \eta))^{-1} \int_0^\infty x^{-1/2} dx \,. \tag{3}$$

In order to calculate $\varepsilon(0)$ and m_x^*, we have employed the $\mathrm{sp^3d^5s^*}$ tight-binding model to calculate the energy band structure for the Si nanowire.[6] Since the maximum density of the state occurs around the Γ-point, one may approximate the electron effective mass by the band curvature at that point.[7] On the other hand, the temperature dependence of the Si lattice constant (a) can be approximated by:[8,9]

$$a(T) = 5.430 + 1.8138 \times 10^{-5}(T - 298.15) + 1.542 \times 10^{-9}(T - 298.15)^2 \,. \tag{4}$$

We have taken the advantage of the similarity of (4) to the dependence of lattice constant on the compressive strain and calculated the temperature dependence of the energy band structure.[10] In doing so, we have used the Harrison law, by which the variation in lattice constant is modeled by the variation in the coupling potential of an atom with its nearest neighbors in the lattice.[11] In the proposed model, the variation in the coupling potential is assumed to be due to the variation in temperature. As a consequence, the Hamiltonian matrix in the tight binding model is modified, accordingly. As a result of this modification the band structure and hence the resulting effective mass should be updated. By inserting the updated values of $\varepsilon(0)$ and m_x^* in (1) and (2), and solving the resultant equations self-consistently, one may update the drain current according to:[12]

$$I = q(Mk_BT/\pi\hbar)[\Im(\eta) - \Im_0(\eta - U_D)] \,. \tag{5}$$

3. Results and Discussion

Using the numerical technique, described in Sec. 2, we have simulated the band structure for a Si-nanowire of diameter 2.75 nm, within the first Brillouin zone, for various temperatures over the range of 50 K $\leq T \leq$ 300 K. Figure 3 compares the conduction sub-bands for $T = 50$ K (dashed-curve) and $T = 300$ K (solid curve), as an example. The inset shown in the figure, illustrates an enlarged portion of the conduction band structure about the center of the Brillouin zone. As seen from this inset, the variation in each sub-band minimum due to the $\Delta T = 250$ K variation in temperature is insignificant. We have also extracted the electrons' effective masses and the energy band gaps at various temperatures. Numerical results indicate that by going from 300 K to 50 K, the electron effective mass increases from $0.271 \times m_0$ to $0.32 \times m_0$, while variations in the energy band gaps are insignificant.

Next, using the effective mass formulation, we have calculated $I_{DS} - V_{GS}$ characteristics of the Si-NW-FET of Fig. 1, for $V_{DS} = 0.4$ V at various temperatures, $T = 50$, 100, 150, 200, 250 and 300 K. Figure 4 illustrates the simulated

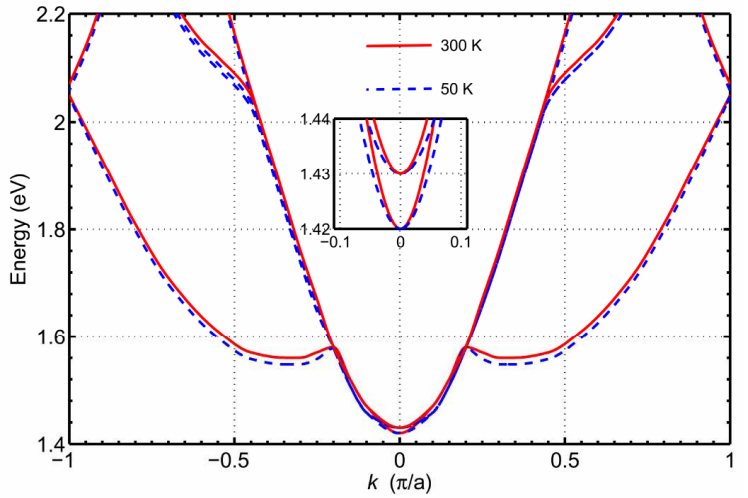

Fig. 3. Comparison of the conduction band structures calculated for a Si-nanowire of 2.75 nm diameter, at two different temperatures. Dashed curves are representing the band structure for 50 K and the solid curves are demonstrating that for 300 K.

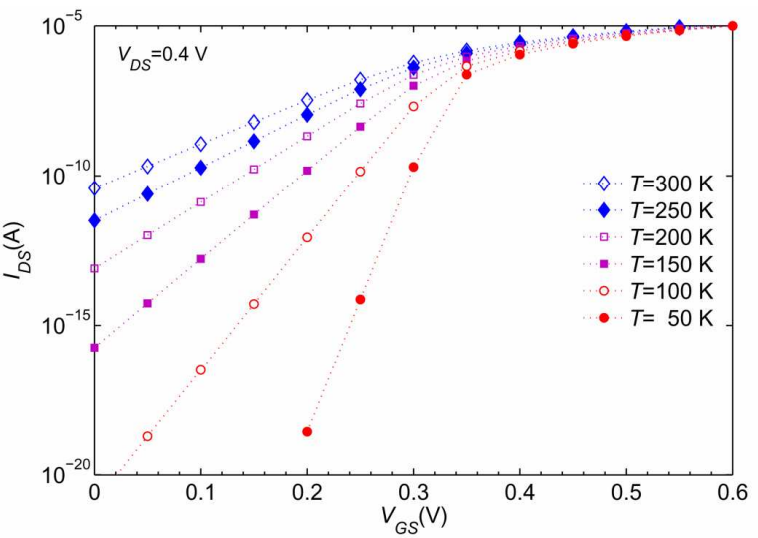

Fig. 4. $I_{DS} - V_{GS}$ characteristics of the Si-NW-FET of Fig. 1 calculated for $V_{DS} = 0.4$ V at various temperatures, $T = 50$, 100, 150, 200, 250 and 300 K.

characteristics. From the slope of the current plot at every given temperature, in the sub-threshold region, one can extract the value of the sub-threshold swing at that temperature using

$$SS|_T = (\partial(\log I_{DS})/\partial V_{GS}|_T)^{-1} . \tag{6}$$

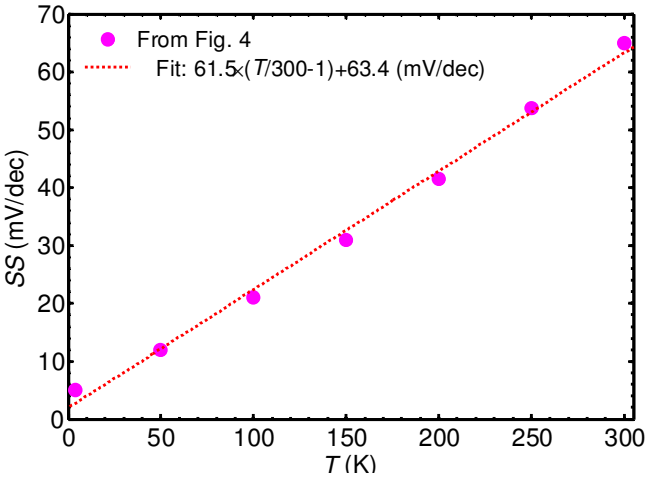

Fig. 5. The temperature dependence of the sub-threshold swing calculated for the device of Fig. 1 (solid circles). Dots represent the linear fit.

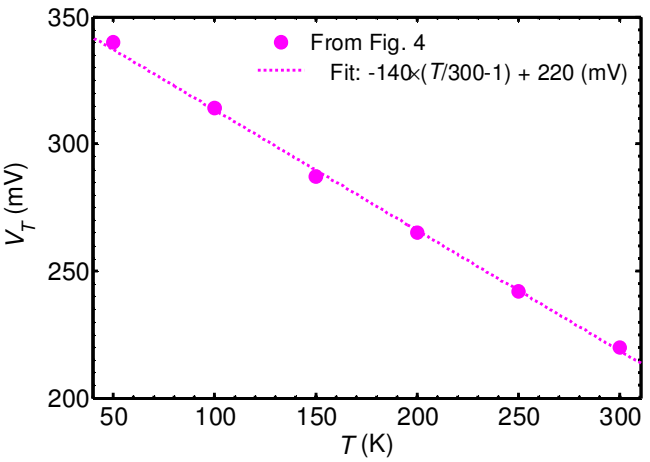

Fig. 6. Temperature dependence of the threshold voltage for the Si-NW-FET of Fig. 1 under $V_{DS} = 0.4$ V, extracted from data of Fig. 4 (solid circles). Dots represent the linear fit.

Figure 5 illustrates the temperature dependence of the sub-threshold swing extracted from Fig. 4 (solid circles).

This figure also demonstrates that a good linear fit (dots), represented by $SS \approx 61.5 \times (T/300 - 1) + 63.4$ (mV/decade), can be made to the calculated data. This might be attributed to sub-threshold currents of the form $I_D = I_0 \exp[q(V_{GS} - V_T)/(nkT + m)]$, in which $n \approx 1.03$, $m = 0.836$ meV and V_T is threshold voltage. This model is also showing that the significantly large difference in the currents, e.g. at 50 K and 100 K are determined by the difference in the values of the exponential

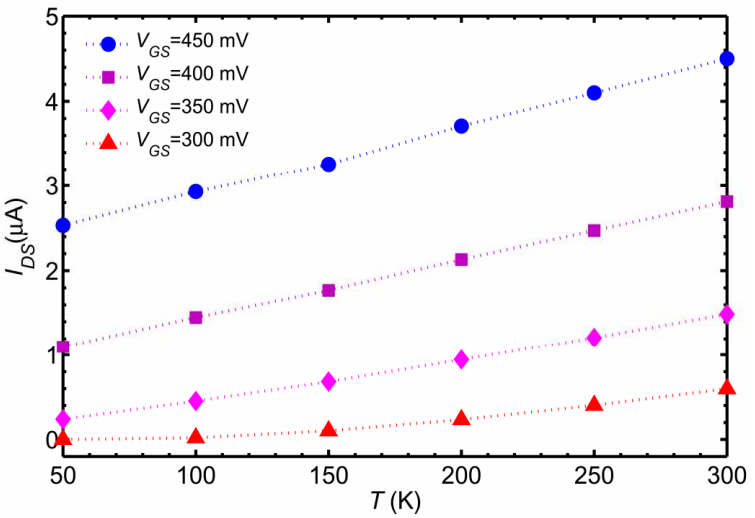

Fig. 7. Temperature dependence of I_{DS}, for the device of Fig. 1, biased in saturation region at $V_{DS} = 0.4$ V and $V_{GS} = 0.3$, 0.35, 0.4, and 0.45 V.

terms at the respective temperatures. Temperature dependency of I_o is based on power law and is not dominant. In other words, the I_D (100 K) and I_D (50 K) are calculated from simulation have full compliance with this model.

The temperature dependence of the threshold voltage, extracted from Fig. 4, is shown in Fig. 6 (solid circles). This figure also illustrates that the extracted data fits excellently to the straight line (dots) represented by $V_T(T) \approx V_T(300) - KT_1(T/300 - 1)$, which in turn is similar to the one used in BSIM4.2.1 MOSFET Model,[13] with $V_T(300) \approx 220$ mV and $KT_1 \approx 140$ mV/K.

Next, we have simulated the I_{DS} versus T for the device of Fig. 1 biased under $V_{DS} = 0.4$ V and various $V_{GS} = 0.3$, 0.35, 0.40 and 0.45 V. Figure 7 shows the plots of the numerical results. This figure shows, except for $V_{GS} = 0.3$ V in the range $T \leq 128$ K (wherein $V_T \geq 0.3$ V), plots of I_{DS} versus T are almost linear with a positive slope that depends on the size of V_{GS}. For a given V_{GS}, the slope $S(V_{GS}) = \partial I_{DS}/\partial T|_{V_{GS}}$ may be defined as the temperature sensitivity of the drain current for that particular V_{GS}. For the figure one can observe that the larger the V_{GS} the more sensitive becomes the drain current to the temperature variation. The calculated values of the slopes, from the plots of Fig. 7, are plotted versus V_{GS} (in the range of 0.3 to 0.45), as illustrated in Fig. 8.

This figure also shows an excellent fit of the extracted data to the parabolic formula represented by $S(V_{GS}) \approx -150 \times (V_{GS} - 0.5)^2 + 8.5$ (nA/K).

Another important parameter, by which one can examine the transistor switching speed, is the device delay time that is defined by $\tau_d = (Q_{\mathrm{ON}} - Q_{\mathrm{OFF}})/I_{\mathrm{ON}}$,[14] wherein Q_{ON} and Q_{OFF} are the amount of electronic charges within the channel in the ON and OFF states, respectively, and I_{ON} is the channel current in

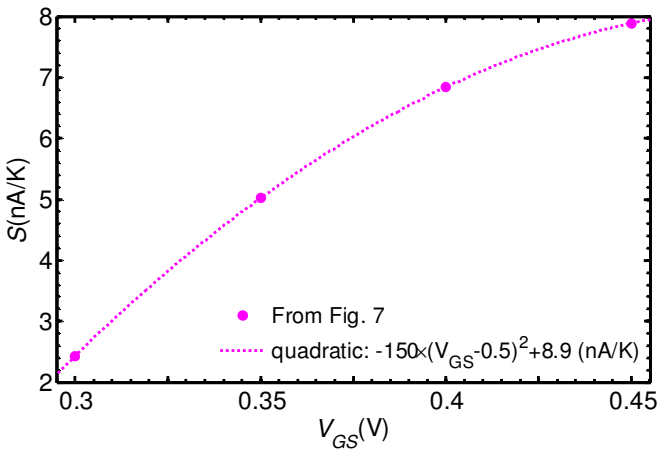

Fig. 8. Sensitivity of the drain current to the temperature ($S = \partial I_{DS}/\partial T|_{V_{GS}}$) as function of V_{GS} for the Si-NW-FET of Fig. 1 under $V_{DS} = 0.4$ V, extracted from the data of Fig. 7 (solid circles). Dots represent the quadratic fit.

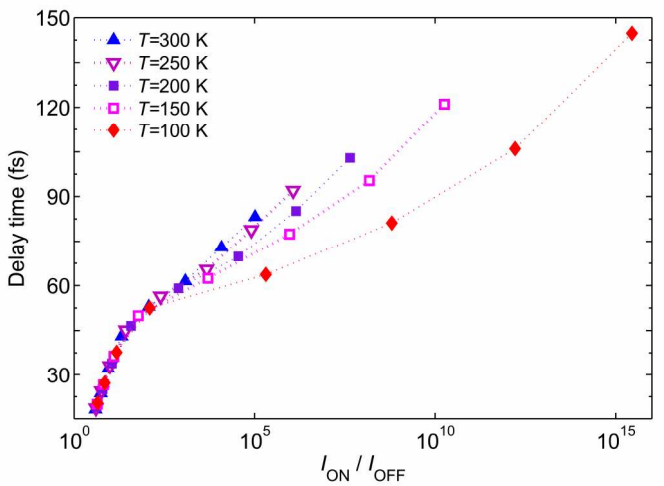

Fig. 9. Delay time versus I_{ON}/I_{OFF} ratio for the transistor of Fig. 1, at $T = 100$, 150, 200, 250 and 300 K.

the ON state. For both ON and OFF states, it is assumed $V_{DS} = 0.4$ V. Plots of the delay time versus I_{ON}/I_{OFF} ratio, calculated at $T = 100$, 150, 200, 250 and 300 K are shown in Fig. 9. This figure shows that for a given I_{ON}/I_{OFF} ratio, as T increases the delay time also increases. On the other hand, comparison of Figs. 4 and 7 reveals that the sub-threshold (OFF) current is more sensitive to the temperature than the ON (saturation) current. That is, as T reduces, I_{OFF} reduces with a much faster rate than I_{ON} does. Consequently, as observed from the figure, for temperatures

as low as $T = 100$ K, $I_{\rm ON}/I_{\rm OFF}$ ratios as high as 10^{15} are achievable, for which the delay time reaches to $\tau_d \sim 145$ fs. Whereas, the highest $I_{\rm ON}/I_{\rm OFF}$ ratio that can be achieved for $T = 300$ K, is about 10^5 leading to maximum delay time of $\tau_d \sim 83.2$ fs.

4. Conclusion

In this paper, we have presented the results of a numerical investigation on the temperature dependence of the electronic properties of cylindrical gate-all-around Si-NW-FET. In this numerical study, we have assumed that the temperature dependence of the Si lattice constant to be similar to its dependence on the strain. Using the tight-binding model we have calculated the energy band diagram of the silicon nanowire. Then, using the numerical values of the electron effective masses and the energy gaps at Γ-point, for various temperatures (50 K $< T \leq$ 300 K) and employing ballistic FET model we have simulated the transistor $I_{DS} - V_{GS}$ characteristics at $V_{DS} = 0.4$ V. Furthermore, we have realized that the extracted values of the sub-threshold swing versus temperature fits to $SS \approx 61.5 \times (T/300 - 1) + 63.4$ (mV/decade), whereas the numerical values of the threshold voltages fits to $V_T(T) = 220 - 140(T/300 - 1)$ (mV), which is similar to that used in the BSIM4.2.1 MOSFET Model. Moreover, by calculating I_{DS} versus T for various V_{GS} and $V_{DS} = 0.4$, we have realized that the drain current in this operating range increases linearly with temperature. By taking the slope of $I_{DS} - T$, for a given V_{GS}, as the sensitivity of the drain current to the temperature we have found that the slopes versus V_{GS} fit a quadratic relation of the form $-150 \times (V_{GS} - 0.5)^2 + 8.5$ (nA/K). Finally, we have calculated the transistor delay times versus $I_{\rm ON}/I_{\rm OFF}$ ratios obtained for various temperatures (100 K $\leq T \leq$ 300 K).

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