A Power and Data Telemetry System for Biomedical Implants

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***Abstract*—This paper describes the design of a power and data telemetry system intended for biomedical implants. The power generation unit utilizes a voltage quadruple, a novel voltage limiter, a new low-power supply-independent voltage reference and a linear voltage regulator. The ASK demodulator uses a high performance comparator based scheme which can recover modulation indices range from 5% up to 90%. Using a 0.18µm CMOS technology the whole system consumes 55µA from the induced power (excluding stimulation current). The system is capable of providing 1.1mA stimulation current under a 3V regulated supply.**

Keywords-power and data telemetry; ASK demodulation; voltage multiplier; voltage regulation; biomedical implants

I. INTRODUCTION

Recently much research has been done on various implantable micro stimulators for different applications. These devices are used for recording neural signals, blood pressure, stimulating cochlear implants, visual prosthesis, nerves and muscles inside the bodies of human or animals [1, 2]. However, to be able to work properly, a power source is necessary for implant's internal circuitry. Thus, the implant may use a battery which required extra room and should be recharged or changed after specific periods [3]. Although batteries have been used in some systems, using inductive links to provide required power wirelessly is a more efficient way [4]. The telemetry procedures used must have adequate power efficiency and data speed. The digital data is encoded and reshaped as a series of pulses, which is sent to the implantable module by amplitude modulation of the carrier [1]. A low carrier frequency usually makes the design simple, while a high carrier frequency will result in a great power loss due to absorption in human tissue. Most carrier frequencies are usually under 20MHz in such a micro system [1]. On the side of human body, demodulating techniques used in the implantable microchips should ensure that the data will not be damaged during data recovery process. As a result, high-performance demodulator circuits are essential.

In this work we have designed the RF interface unit of an implantable device including power extractor and amplitude-shift keying (ASK) demodulator. In section II, we introduce the overall design of the power supply and ASK demodulator unit embedded in the micro stimulator system along with details of the circuits. In section III we express the results of simulations and section IV presents the conclusion.

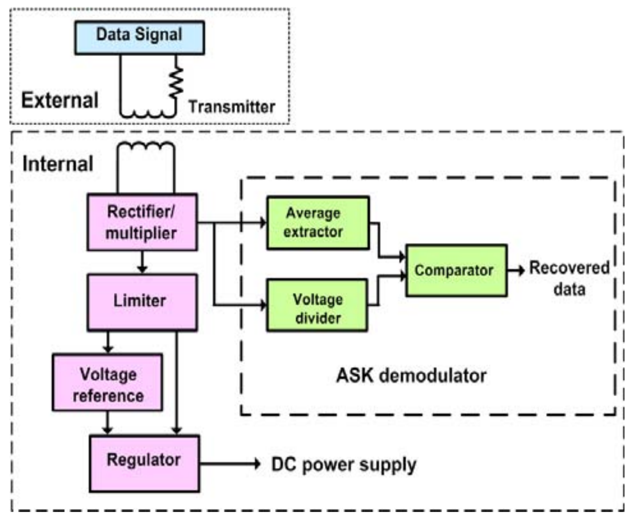

Fig. 1. Block diagram of the designed system

II. SYSTEM ARCHITECTURE

Fig. 1 shows block diagram of the power supply and ASK demodulator units of a micro-stimulator system. The mutual inductance has been used for transferring power from outside of body to inside. The internal unit contains two parts: the DC supply voltage provider and ASK demodulator. The supply unit includes a voltage limiter, a voltage rectifier/multiplier, a voltage reference generator and a voltage regulator. An average extractor, a voltage divider and a comparator are used for demodulating induced ASK modulated signal. Following parts describe each circuit block in more detail.

A. *Voltage rectifier/multiplier*

Fig. 2 shows the schematic of the voltage rectifier and multiplier. In this work, we have employed half-wave rectifier to have small chip area. The structure contains four pairs of MOS transistors and capacitors. The output is an unregulated dc voltage with ripples which has used for biasing the other parts. Voltage multipliers are used mostly to develop high voltages where low current is required [5]. In this design, the peak of the input voltage has been increased four times in the

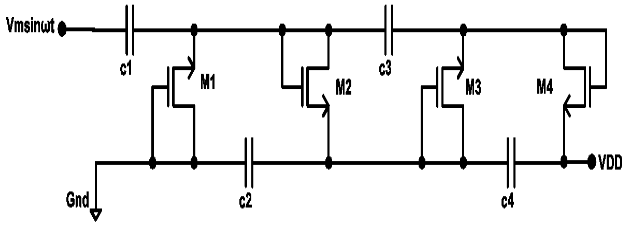

Fig. 2. Voltage rectifier/multiplier circuit

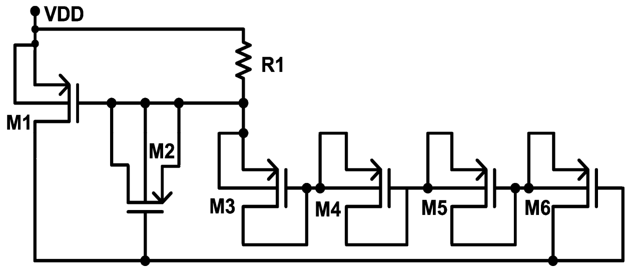

Fig. 3. Voltage limiter

output. The capacitors also charge in positive and negative cycle of the input signal. In this circuit, the diode-connected nMOS transistors, M1, M2, M3 and M4 do the job of rectification [6].

B. Voltage limiter

In the case of power telemetry by coils which coupled inductively, according to different applications the distance between internal and external coil may be variable. If the distance between these coils is decreased, a relatively high voltage may be induced to the internal coil. Thus, the internal parts need protecting to prevent damage from the high voltage, therefore a voltage limiter circuit is required.

As shown in Fig. 3 the output of voltage multiplier (VDD) is compared with series threshold voltages of M3-M6. When the voltage over R1 reaches to a specific value, M1 turns on and begins to conduct the current. When the load current of the rectifier goes up, its output voltage will be dropped. Hence, VDD can be adjusted not to be higher than the safety level of internal circuitry.

C. Voltage Regulator

Fig. 4 shows the circuit schematic of voltage regulator where an nMOS input operational amplifier (OPAMP) is used to achieve required input dynamic range. The negative feedback is recognized by R1 and R2 and pMOS transistor, M1, is the pass transistor which supplies the total required current of the whole chip. The voltage regulator receives the output voltage of the rectifier and adjusts it to a steady 3-V dc with 0.1V ripple to supply other parts of the implantable device. This regulator must supply minimum 1mA to the stimulating electrodes. In this circuit the output of voltage regulator is:

$$Vreg = Vref\,(1+\frac{R_2}{R_1}) \qquad (1)$$

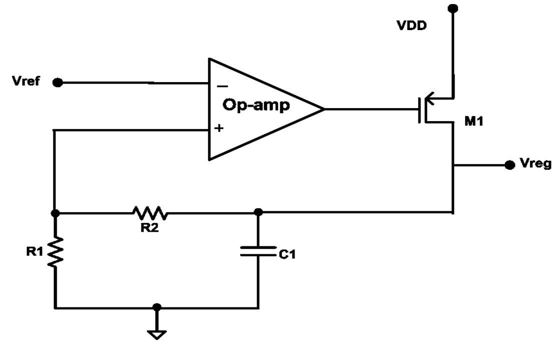

Fig. 4. Voltage regulator circuit

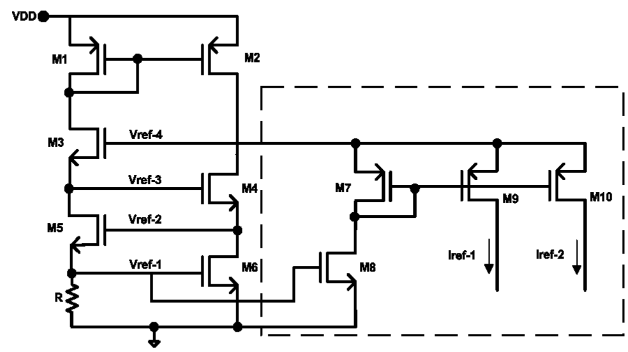

Fig. 5. Supply independent reference circuit

where V_{ref} is the reference voltage which has been generated by supply independent reference circuit.

D. Reference Circuit

Well known multiple output supply independent voltage reference circuit has been commonly used in biomedical implant systems [7], [8]. As shown in Fig. 5, we recommend an improved version of the circuit to provide multiple supply independent current reference. The transistor M8 receives its gate bias from Vref-1 and specifies the reference current of the current reference part. Any other required reference current will be a scaled replica of the current flowing in M8 and M7. However, all the main reference current and its replicas will be sunk by M2. So, M2 should be sized properly in order to be able to supply the current needed for both voltage reference and current reference circuits as follow:

$$\left.\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right|_{old} = \frac{I_2}{I_1} = \frac{I_4}{I_1} \qquad (2)$$

$$\left.\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right|_{new} = \frac{I_2}{I_1} = \frac{I_4 + I_{tot}}{I_1} \qquad (3)$$

$$\left.\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right|_{new} = \left.\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right|_{old} + \frac{I_{tot}}{I_1} \quad (4)$$

where the terms "new" and "old" refer to the reference circuit with and without current reference part, respectively. I_1, I_2 and I_4 denote the drain current of the M_1, M_2 and M_4, respectively, and I_{tot} stands for the total current sunk by current reference part.

E. ASK Demodulator

Fig. 6 shows the ASK demodulator, consisting of a low pass filter network as average extractor, a voltage divider circuit, and a comparator with internal hysteresis and a buffer. No envelope detector is needed in this scheme since the rectifier has already done the job. The rectified voltage will be delivered to the voltage divider and then will be compared with its average generated by the average extractor. In order to diminish the undesired effects of high frequency ripples of rectifier's output on demodulator operation, a comparator with hysteresis is incorporated.

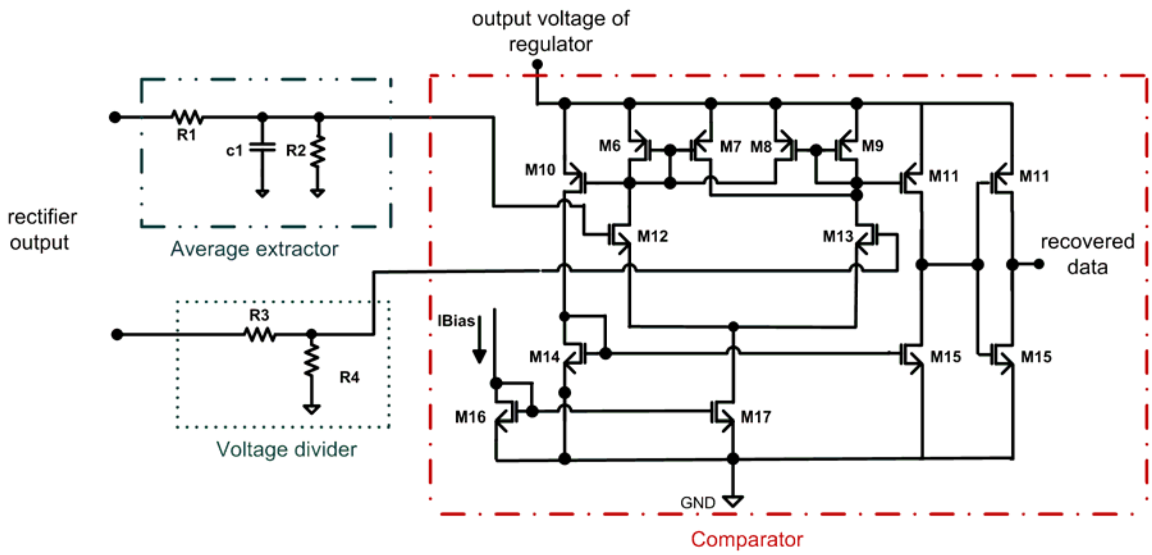

Fig. 6. ASK demodulator circuit

III. SIMULATION RESULTS

The proposed fully integrated circuit blocks have been designed and simulated using a 0.18µm CMOS process. With a 10 MHz carrier frequency, the system can provides a data rate of 250 Kbps and tolerates a modulation index from 5% to 100%.

The dependence of the regulator output (Vreg), and the reference voltage (Vref1), upon the rectifier output (VDD) variations is depicted on Fig. 7. According to this figure, the line regulation of the regulator is about 21mV/V while Vref1 shows only 0.8% variations. The current reference generated by supply independent reference circuit is shown in Fig. 8 where its dependency on the supply is calculated to be approximately 10%.

Fig. 9 presents the simulated waveforms of the inputs to the desined ASK demodulator. The voltage devider output has a 40mV ripple for a received ASK signal with 5% modulation index. The RC low-pass filter of average extractor has a moderate time constant to prevent large value elements and save area. The output of the demodulator is given in Fig. 10 as a rail-to-rail digital-level recoverd data.

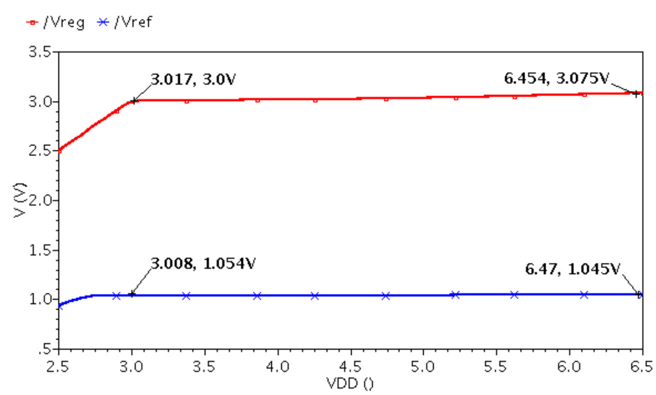

Fig. 7. Output of the voltage regulator (Vreg) and reference voltage generator (Vref) in response to VDD variations

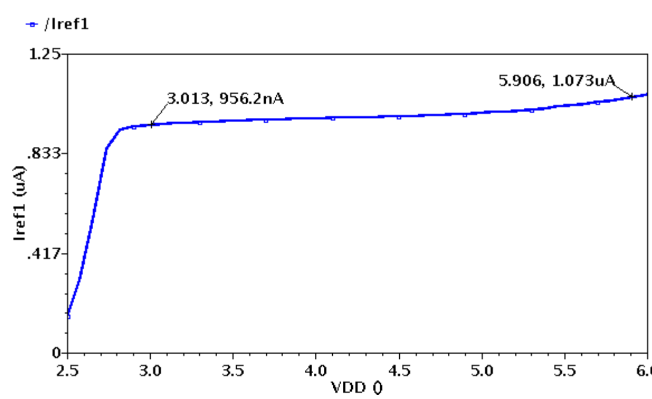

Fig. 8. Output of the current reference (Iref1) in response to VDD variations

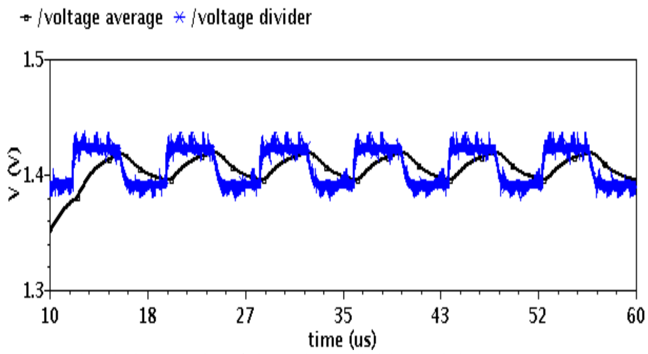

Fig. 9. Simulation results of the voltage divider and the average extractor

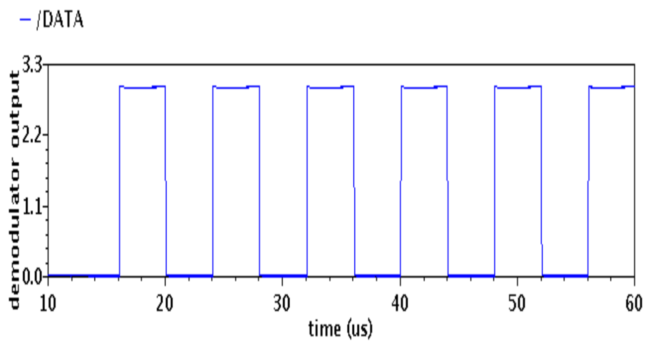

Fig. 10. Output of the ASK demodulator (recovered data)

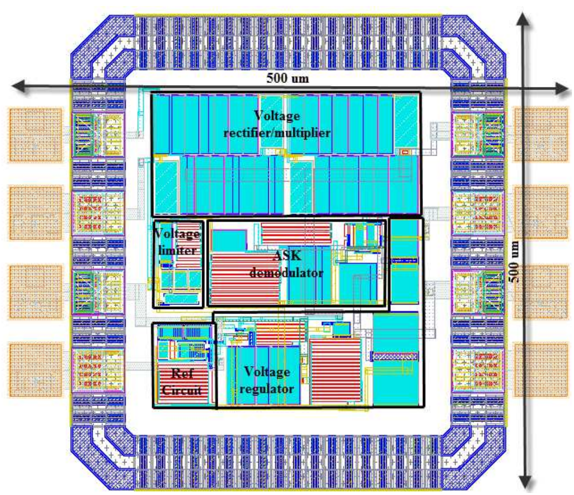

Fig. 11. System layout

The system layout is shown in Fig. 11. The chip area including the signal and test pads is about 0.25mm^2. The overal specifications of the system have compared with some recently published litrature and summarized in Table I. The circuit reported here has a relatively low power consumption for a nominal 10MHz carrier frequency and 250Kbps data rate.

IV. CONCLUSION

A power extractor and data demodulator for biomedical implants was reported. Operating with a 10MHz carrier frequency, the system has 110µW power consumption for a 250Kbps data rate. Using efficient architectures for the system blocks, a robust functionality along with low power consumption is achieved. Simulation results confirmed operability of the system.

TABLE I. Specifications of the system

papers	Ref[1]	Ref[2]	Ref[9]	This work
Technology	0.35µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Regulated supply voltage (v)	3	1.8	1.8	3
Carrier frequency (MHz)	2	0.25	2	10
Demodulation	ASK	ASK	ASK	ASK
Data rate (Kbps)	1000	NA	1000	250
Modulation Index (%)	NA	NA	2.86-38.64	5-90
Power consumption (mW)	2.25	NA	0.396	0.11
Area (mm2)	2	NA	3.6e-3	0.25

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----------------------- REVIEW ۱ ---------------------
PAPER: ۷۳
TITLE: A Power and Data Telemetry System for Biomedical Implants
AUTHORS: Sima Ghandi, Mehdi Lotfi Navaii and Mohsen Jalali

OVERALL RATING: ۱ (weak accept)
REVIEWER'S CONFIDENCE: ۲ (medium)

This paper shows a good approach to implantable telemetry system in terms of power and data.
۱) In part II.B. voltage limiter
"In the case of power telemetry by coils which ~~~~ a voltage limiter circuit is required." => need references here
۲) OPAMP is used to achieve required input dynamic range. => How much dynamic range?
۳) Figure ۷,۸,۹,۱۰, are they simulation results in schematic or post-layout?
If schematic simulation, how about using post-layout simulation results?
۴) In table I, replace "papers" => "Parameters"

----------------------- REVIEW ۲ ---------------------
PAPER: ۷۳
TITLE: A Power and Data Telemetry System for Biomedical Implants
AUTHORS: Sima Ghandi, Mehdi Lotfi Navaii and Mohsen Jalali

OVERALL RATING: ۱ (weak accept)

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