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# Reliable energy-aware application mapping and voltage–frequency island partitioning for GALS-based NoC

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ABSTRACT

Reliable energy-aware application mapping, task scheduling, and voltage–frequency island partitioning so as to minimize the energy consumption while preserving the required bandwidth and latency is considered as a challenging problem in the designing of Multi-Processor System-on-Chip. To achieve modular design and low power consumption, Globally Asynchronous Locally Synchronous (GALS) design paradigm is a promising approach which fits very well with the voltage–frequency islands concept. In this paper, we formulate mapping problem of a real-time application with stochastic execution times onto multicore systems, scheduling tasks on processors, and assigning voltage–frequency levels to Processing Elements (PEs) as a Mixed Integer Linear Programming (MILP) in GALS-based Network-on-Chip. Furthermore, owing to the importance of reliability issue, we address the effects of transient faults in our proposed MILP formulation such that the reliability of the whole system incorporating several heterogeneous PEs is guaranteed to be better than a given threshold. Due to the *NP*-hardness of such a problem, a rounding by sampling-based heuristic algorithm is provided. Experimental results based on E3S benchmark suite and some real applications show the effectiveness of our proposed heuristic in achieving a near-optimal solution in a small fractional of time needed to find the optimal solution. Experimental results also show that, our formulation preserves the required reliability and increases the energy consumption by 70% in some cases.



## 1. Introduction

Due to the increasing demand for high computational capabilities, Network-on-Chip (NoC) has been emerged as a promising interconnect solution to achieve high performance systems [2]. Such chips consist of regular tiles and contain variety number of PEs. The PEs can be DSP cores, programmable general purpose cores, high-bandwidth Input/Output (IO) devices or task specific coprocessors which introduce heterogeneity within the chips. The NoC provides more scalability, flexibility, and performance over the bus-based communication mechanism [3]. Developing a design methodology for NoC-based multiprocessor System-on-Chip (MPSoC) while optimizing the total system energy consumption under the bandwidth, latency, and reliability constraints poses novel and exciting challenges to the research community [4].

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