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Intricacies in Digital CMOS Implementation of a Reconfigurable Fuzzy Logic Traffic Light Controller

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Abstract—**In this paper, the procedure of CMOS design of a reconfigurable fuzzy traffic light control that may work in a severe condition is discussed. The chip receives the membership degree parameters and traffic density indexes. The membership degree is allowed to have variable numbers of reconfigurable trapezoid patterns. Import/export of data is carried out through a serial link. The chip is designed using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) implementing an optimized fuzzy traffic controller developed in [1]. Based on the traffic density, the algorithm decides whether to terminate the current green phase or to extend it for some more time for better intersection traffic handling. Design is tested versus full software implementation of the algorithm. The result exhibits successful hardware implementation. Then, the layout of the chip based on minimum die area is also derived.**

Keywords-Fuzzy logic; Traffic light control; Fuzzy CMOS implementation; VHDL;

I. INTRODUCTION

The key benefit of direct hardware implementation of an algorithm is better integrity, better performance, higher reliability, lower cost and reduction of hardware overhead. A circuit board is compacted to a chip, various elements come together and the number of wirings is reduced. One of the candidate systems is surely traffic controller when it is produced in industrial-scale.

Traffic management in most intersections has been fixed and pre-programmed which does not consider real-time traffic fluctuations. In the past few decades, researchers have proposed various control models to improve the traffic capacity of crossroads. In this respect, the classical adaptive methods have been proposed [2] and, later, other choices such as resorting to the artificial intelligent methods: fuzzy logic and neural network have gained momentum. A fuzzy logic-based traffic controller for a four-approach isolated intersection with through and left-turning movements using two stage fuzzy controllers is proposed in [2]. Optimizing the fuzzy strategy using genetic algorithm is the result of a try in [1] showing that it outperforms the preceding schemes.

The software execution of a fuzzy controller is straight-forward; however, at least it needs a single board computer. Compact specific hardware implementation enjoys reliability for a system that works in a severe environment and lower cost even in industrial-scale fabrication. In this respect, in [3] a review of attempts in VLSI implementation of fuzzy controllers for various applications is presented. Analog, digital CMOS and FPGA (Field Programmable Gate Array) [4, 5] implementation have been examined in various investigations. The objective of the designs is usually small silicon die, high speed of operation and adaptability to different applications. Iin case of fuzzy logic traffic control, however, the most desired one is compactness, less die area and re-configurability as the parameters of the algorithm of the design may vary as new suggestions are emerged.

In this paper, a special digital CMOS Fuzzy Logic Traffic Controller (FLTC) is designed. It is reconfigurable and has the capacity of containing the entire fuzzy algorithm, while minimization of the number of pins and die area are the main objectives. Traffic is simulated using MS Visual C# (main program), and traffic data are transferred to the CMOS chip simulator, Modelsim (Alera Co), where fuzzy traffic control strategy is applied. The output, then, switches the traffic lights, as it should be, to optimize the vehicles commutation. The simulation results are compared with what full software implementation exhibits. Similarity between the results, indicate that the design objectives has successfully been accomplished. Moreover, the layout of the CMOS chip using SOC Encounter of Cadence SOC Encounter, is also derived.

In section 2, an isolated intersection and its parameters are introduced. The hardware requirement of a FTLC is discussed in section 3. The simulation setup is elaborated in section 4. Section 5 details the CMOS layout of the hardware implementation and lastly, the conclusion comes in section 6.

II. ISOLATED INTERSECTION PARAMETERS

Fig. 1 shows a three-lane cross road. It is assumed that the vehicles arrive at right lane turn right, at middle lane proceed straight forward and at left lane turn left or perform U-turn. Each lane has two detectors, one at the intersection that counts the passing traffic and the other, far from the intersection (upstream) detecting the approaching traffic.

For the purpose of traffic management, 4 transit phases [1, 2] are considered as it is shown by arrows in Fig. 1 as follows:

Phase1 (P1): Green light for East-West left and/or U-turn;