# Single chip digital CMOS implementation of a reconfigurable fuzzy logic traffic controller

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**Abstract:** In this paper, single chip CMOS design of a reconfigurable fuzzy traffic light controller is studied. The chip inputs are traffic data and parameters of fuzzy membership degrees (MD). MD's are allowed to have variable numbers of reconfigurable trapezoidal membership functions. Based on the traffic density, the fuzzy traffic controller decides either to terminate the current green phase or to prolong it for better intersection traffic handling. Import/export of data and working parameters are carried out through a serial link. The chip is designed using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) and its layout is derived using SOC Encounter. Parallel and sequential architectures for fuzzy processing which have diverse impacts on the chip area (cost) and fuzzy process delay (speed) are evaluated. The design of choice is a sequential architecture maintaining low power, low die area (cost) and adequately fast speed, to be capable of containing the entire fuzzy traffic control and data collection hardware. The simulated chip performance is tested versus full software implementation of the algorithm.

**Keywords:** Fuzzy logic, traffic light control, CMOS design, VHDL

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