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Research Article

Optimal ILP-Based Approach for Gate Location Assignment and Scheduling in Quantum Circuits

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Physical design and synthesis are two key processes of quantum circuit design methodology. The physical design process itself decomposes into scheduling, mapping, routing, and placement. In this paper, a mathematical model is proposed for mapping, routing, and scheduling in ion-trap technology in order to minimize latency of the circuit. The proposed model which is a mixed integer linear programming (MILP) model gives the optimal locations for gates and the best sequence of operations in terms of latency. Experimental results show that our scheme outperforms the other schemes for the attempted benchmarks.

1. Introduction

Quantum effects have been a major concern in classical computers in metal-oxide-semiconductor technology (CMOS) as the feature size shrinks into the 10 s of nanometers range [1]. Quantum effects such as entanglement and superposition are amplified in quantum computers. They operate on the entangled superposition states and this is where the power of quantum algorithms comes from.

A quantum circuit is a model for quantum computation. In a large picture, the quantum circuit design flow includes two main tasks: synthesis and physical design (Figure 1). The physical design consists of scheduling, mapping, and placement processes. In this paper, an ILP-based approach is proposed for scheduling, routing, and mapping processes. The proposed approach takes an initial netlist and a layout, and maps and schedules the gates on the layout.

A quantum circuit is defined as a sequence of quantum operations acting on one or multiple qubits. These operations could be categorized in two groups: (1) single or multiqubit logical gates and (2) single qubit measurement. In this paper, only one- and two-qubit operations are considered due to some practical limitations on many quantum circuit technologies [2].

Ion-trap technology is a quantum technology where every universal element for quantum computation has been realized with a clear scalable communication model [3, 4]. In this technology, an ion is the physical demonstration of a qubit and a gate location is a location wherein a gate is performed. Each ion could be trapped or physically moved between traps by applying pulse sequences to discrete electrodes (Figure 2). Each qubit is measured by stimulating the target ion with a different frequency laser pulse [5].

In this paper, library of macroblocks which is defined in [6] (Figure 3) is used due to two major advantages. The main reason is that by using this library, some low level details could be removed and it is not necessary to consider the variations in ion types, size of electrodes, and precise voltage levels needed for trapping and moving ions. All of these details are condensed within the macroblocks [7, 8].

In this library, a 3×3 structure of trap regions and electrodes forms each macroblock. Each structure has some ports to allow qubits to move between the macroblocks. Gate locations are indicated by black squares. Various orientations of each macroblock could be used in a layout.

The paper is continued as follows: an overview of the prior work is presented in Section 2, followed by the details of the proposed model in Section 3. An illustrative example