

# Design and VLSI Implementation of New Hardware Architectures for Image Filtering

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**Abstract**— Nowadays, hardware implementation of image and video processing algorithms is highly attractive. Needing to real-time processing makes hardware implementation of these algorithms inevitable. In most of image and video processing algorithms, pre-processing filters are the first and most important stage of the algorithm. In this paper, we propose new hardware architectures for the implementation of image filters including Gaussian, median and weighted median filters. The proposed architectures aim to optimize the filter implementation for speed and gate usage. The proposed architectures are implemented and synthesized in ASIC with 65nm technology and different specification of the implementation such as maximum clock frequency and IC area are reported.

**Keywords**— Gaussian filter; Median filter; Weighted Median filter; hardware architecture; ASIC implementation; Real-time processing;

## I. INTRODUCTION

Due to the innate flaw of the imaging systems, quantization effect and the noise of recording devices, images and video frames are subjected to noise. Noise reduces the image quality and consequently the performance and efficiency of subsequent processing algorithms such as edge detection, corner detection and image segmentation will be negatively affected [1, 2]. Therefore, it is necessary to remove or reduce the image noise before applying the main algorithm.

Various models are used to describe image noise based on its origin and the probability density function such as Gaussian, impulsive, uniform, Erlang and power-line noise. Based on the noise type and its effects, different algorithms are also used for image filtering. The noise smoothing filters are generally classified in two groups: linear and nonlinear filters. In linear filters like Gaussian filter, filtering operator is linear, while non-linear filters apply a non-linear function to the image windows. Median and weighted median filters are examples of the mostly used non-linear filters.

Recently, hardware implementation of image processing algorithms has emerged as the most viable solution for improving the performance and the speed of the different image processing algorithm [3, 4]. Hardware implementation

of the filtering algorithms using parallel and pipelined architectures is also a proper solution to ensure higher accuracy and higher update rate. Most of the hardware implementation of image filtering algorithms focused on median filtering. In [5] a hardware architecture was proposed for the implementation of a  $3 \times 3$  median filter. Hu and Ji proposed two different architectures for hardware implementation of median filtering including standard and multi-level median filters [2]. The pipeline architecture of multi-level median filter needs 4 clock cycles of latency in comparison with the 6 clock cycles for the standard median filter. However, a multi-level implementation can not calculate the median value for all the intensity values. In [6] an optimized systolic array was utilized for hardware implementation of median filtering. The pipeline structure of this architecture requires 7 clock cycles to calculate the median value.

There are two types of technologies for hardware design including 1- full custom hardware design that is well known as Application Specific Integrated Circuits (ASICs) and 2-semi custom hardware design, which includes programmable devices such as Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs) [2, 7]. DSPs are special purpose CPU and reconfigurable devices. These devices generally do processing in serial and suffer from non-pipeline implementation of the image processing algorithms. Although FPGAs are more general for different hardware architectures, ASICs have the advantage of less area and higher speed [8].

In this paper, we present new hardware architectures for the implementation of image filtering. Gaussian, impulsive and salt & pepper noises are the most common source of noise in images. Gaussian and median or combined Gaussian and median filtering also called weighted median filtering are the mostly used algorithms to handle these kinds of noise sources. Therefore, three hardware architectures for the implementation of Gaussian, median and weighted median filters are proposed. We evaluate the accuracy of the proposed architectures by comparing the results of software and hardware implementation and report different ASIC parameters.

The paper is organized as follows: in section 2, we introduce Gaussian, median and weighted Median filters. In section 3, we present the proposed hardware architectures for