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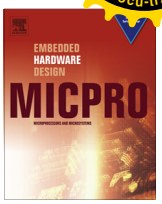

FREE papers

Scenario-based quasi-static task mapping and scheduling for temperature-efficient MPSoC design under process variation

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ABSTRACT

Nowadays, employing the worst case analysis is the most common approach to provide unified static task mapping–scheduling plans on MPSoCs. Since the whole design space nor a subset of design space are not explored in the worst case methods, these approaches may fail to achieve efficient performance yield. In this paper, we present a temperature-aware quasi-static task mapping–scheduling framework under process variation for hard real-time and periodic systems on MPSoCs. By employing the stochastic optimization and scenario-based approaches, we explore a few representative scenarios in the whole design space of the chip using the probability density function of the problem random variables. Then, we obtain a compact set of near optimal mapping–scheduling of real-time tasks which targets performance-yield maximization and minimization of the expected values of peak temperature. Consequently, considering different chip parameter configurations, we construct the plan set as the solutions that attain the best variation-aware task mapping–scheduling that satisfy the deadline and minimize the temperature. This plan set can readily look up at run time by the system scheduler of the chip to find the proper plan of the tasks based on the run-time parameters. The experimental results demonstrate significant improvements in performance-yield and peak temperature for almost all of the test cases off homogenous and heterogeneous MPSoCs.

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1. Introduction

Technology scaling of transistor features enables the integration of multiple heterogeneous processors on a single die, known as Multi-Processor Systems on Chip (MPSoC). This aggressive scaling may lead to higher power density and temperature and in turn causes a localized high temperature region known as thermal hot spots. Thermal hot spots have adversarial effects on the operations of the chip such as:

- Decreasing the reliability: Failure scenarios such as Electro-migration and Hot carrier Injection increase by growing thermal hot spots [1]. According to [2], a change of operating temperature by 10–15 °C results in a 2*X* difference in the lifespan of devices. Moreover, the thermal expansion, especially at hot spots, may lead to uneven chip expansion and as a result potentially breaks the chip physically.
- Increasing power consumption: Temperature induces a positive feedback with leakage power consumption. This leakage may account for up to 60% of the total energy consumption in deep sub-micron technologies [3].

Consequently, temperature has become an issue of paramount value due to its direct or indirect role in power consumption, reliability, and cooling cost, so it should be considered at the early phase of the design of MPSoCs.

On the other hand, continued scaling of deep sub-micron technologies reveals some new challenges such as soft errors, device aging and process variation [4]. Herein, process variation exacerbates chip design process by imposing uncertainty in key parameters of the transistor such as channel length, gate-oxide

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