A Dimmable Electronic Ballast for CFLs Compatible with Phase-Cut Dimmers

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Abstract— **In this paper a new dimmable electronic ballast circuit compatible with available commercial phase-cut dimmers for compact fluorescent lamps (CFLs) is proposed. Proposed circuit has considerably low cost and controls the output light linearly with high power factor (PF) in the whole dimming firing angles. In the proposed dimming circuit, desired firing angle convert into power switch duty cycle with a linear relation. Power switch duty cycle controls the DC-Link voltage and the output power is determined by this voltage. In this paper operation of the proposed dimming circuit along with duty cycle variation following firing angle variations has been explained. To explore the feasibility of proposed circuit, a 42 Watts CFL was tested under a laboratory prototype of proposed circuit.**

Keywords- Electronic Ballast; CFL; Dimmer

I. INTRODUCTION

Compact fluorescent lamps (CFLs), due to their more lifetime and higher efficacy over conventional incandescent lamps are widely in use. Electronic ballasts are preferred to magnetic ballasts in CFLs due to their low weight and volume, high power factor (PF), high efficiency, dimming capability and lower flickers and noises[1-2]. Regular CFL ballasts comprise a diode rectifier and a half bridge resonant inverter which suffers from low input power factor [3-4]. This feature becomes worse when the lamp is dimmed. To meet the IEC 61000-3-2 standard [5] which determines input current harmonic limitations, a power factor correcting stage should be added to the regular ballasts.

Various small size, low cost electronic ballasts are proposed in [6-7]. To comply with energy saving requirement, dimming capability should be provided in the electronic ballasts. Dimming capability can be accomplished by duty cycle control, switching frequency control, phase-shift control and DC-Link voltage control [8, 9].

Duty cycle control has a narrow light control capability, which has prevented it from turning into commercial use [8]. Frequency control of resonant converter is widely in use. Following frequency variations, input impedance of resonant converter varies. In this case the transferred energy to the lamp would be controllable [9]. This approach suffers from complicated EMI filter design. In phase-shift dimming, lamp energy can be controlled through changing the phase difference between input voltage and current of the resonance inverter. The most appropriate way to control the lamp light is the controlling of DC-Link voltage applied to the resonant stage at a fixed frequency. Using the phase-cut dimmers of without the need of additional wiring is discussed in [10-11]. Phase-cut dimmers in commercial CFLs cause a low PF at the input of the ballast. Moreover in higher firing angles, phase-cut dimmers result in a visible flickering and small output light controlling.

In this paper a new dimming method based on both power switch duty cycle and firing angle control of dimmer is proposed. The proposed dimming method features high PF in the whole controlling range. Furthermore the proposed dimming method features low cost and small size which provides the feasibility of fitting it into a CFL base. To explore the validity of presented analysis and design, proposed dimming circuit was tested for a 42 watt CFL. This paper organizes as follow: section II and III explain the power stage and control circuitry of proposed dimming circuit respectively. Section IV deals with operation of dimming circuit and section V presents the experimental and simulation results of proposed dimming circuit under firing angle variations to verify the analysis and design.

II. POWER STAGE OPERATION

The power stage of dimming circuit is a high PF, single switch topology presented in [12]. Moreover the power switch of the topology experiences lower voltage and current stresses compared with other topologies [6-7]. Fig. 1 depicts the power stage of the dimming circuit. The power stage comprises a SEPIC converter as a PFC stage and a single-switch current source resonant inverter. As shown in Fig. 1, SEPIC converter in the PFC stage, consists of L_{PFC} ,C_1 ,L_1 ,C_{DC} ,D_{OUT} ,D_{PFC} and common switch M_1. Current source resonant inverter components are L_{in} ,C_r ,L_r ,D_r ,common switch M_1 and L_P for high ignition voltage at the starting instances. Several advantages of the proposed topology over other topologies can be listed as high PF due to PFC stage, low switching losses due to inherent ZCS circuit technique, simple EMI circuit design due to fixed frequency performance and reasonable crest factor (CF).

Fixed frequency, Discontinuous conduction mode (DCM) operation of SEPIC converter results high PF at the input of the ballast. Ballast designing procedure was presented in [12].

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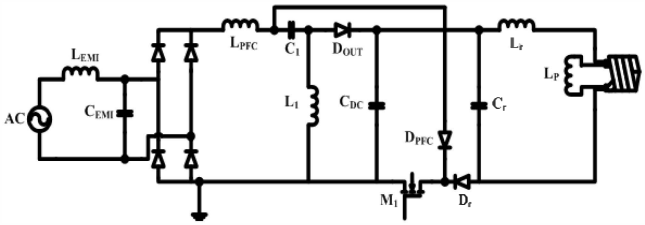


Figure 1. Power stage electronic ballast

III. DIMMING CONTROL CIRCUIT DESCRIPTION

Fig. 2 shows the proposed block diagram of dimmable CFL ballast with phase-cut dimmer. Fig. 3 shows the proposed dimming control circuitry. Proposed dimmable ballast provides linear output light control through all firing angles and the light can be reduced to a great deal (equivalent to 5% of output power) while high PF would be achieved even at low output power.

In the proposed dimmable ballast, input voltage would be sampled and then applied to the duty cycle control circuitry. Lamp output power would be controlled DC-link voltage via duty cycle control. As shown in Fig. 2, sampled line input voltage would be compared with a small DC voltage ($-V_{dc}$ and $+V_{dc}$) to detect the firing angle "α" generated by phase-cut dimmer. If this small DC voltage is lower or larger than the sampled AC input voltage, a square pulse signal with line frequency would be produced at the output of comparators (V_c). Fig. 4 shows the waveforms of control circuit. If the "α" firing angle applies to the phase-cut dimmer at t_0, cut-off time of V_{in} would increase. In this case pulse width produced at the output of comparators reduces, and then the pulse width would be a linear function of firing angle "α". To stabilize the control circuitry, a PI controller is added to integrate RC net output. The integrator output would be compared with a saw tooth waveform and consequently PWM switch gate would be produced.

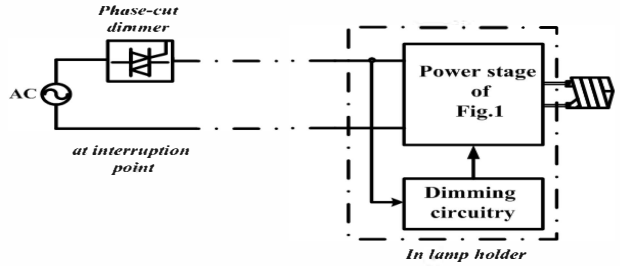


Figure 2. Phase-cut dimmer and dimmabale CFL.

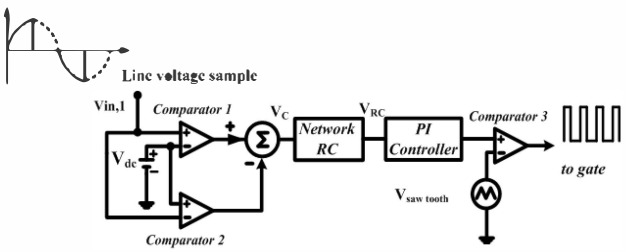


Figure 3. Dimming circuitry as ballast PWM control unit.

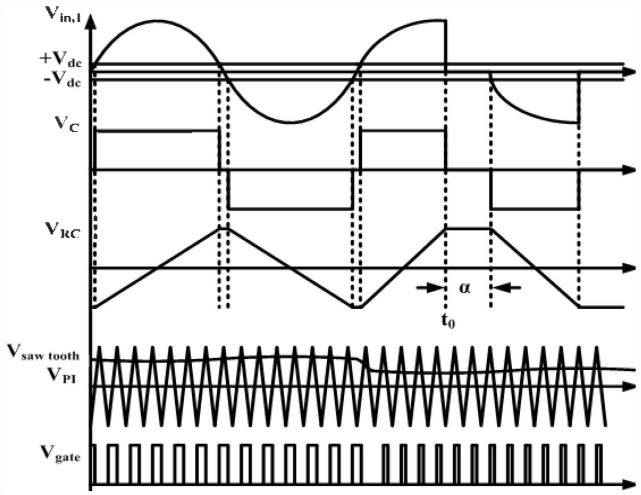


Figure 4. Dimming circuit waveforms

In the control circuit, output of RC net (V_{RC}) remains symmetry with firing angle variations. In this case the control circuitry remains stable through all firing angles of dimming. The purpose of using simultaneous duty cycle and phase-cut dimmer control is preventing full dimmer usage in output power controlling. In this case a shorter range of phase cutting is used (approximately 90^0) and consequently a high PF would achieve.

IV. OPERATION OF THE PROPOSED DIMMING CIRCUIT

Increasing firing angle of dimmer from 0 to π radians, changes the duty cycle of power switch from its maximum at the full power to its lowest dimming condition. SEPIC converter output voltage drop due to duty cycle reduction, reduces the input power of current source resonant inverter which is the same as the lamp power. Duty cycle as a function of firing angle can be achieved by ignoring SEPIC converter losses as (1):

$$P_{o,avg}(\alpha) \approx V_{dc}(\alpha) I_{dc}(\alpha) = P_{i,avg} \quad (1)$$

In which $P_{o,avg}$ is the average output power of SEPIC converter, V_{dc} is average of DC-Link voltage, I_{dc} is the averaged output current of SEPIC converter and $P_{i,avg}$ is the averaged input power of SEPIC converter. DC-Link voltage as a function of firing angle can be expressed as:

$$V_{dc}(a) = \frac{1}{G}\left(G\, V_{dc,max} - \frac{\alpha K}{\pi}\right) \quad (2)$$

In which K and G are multiplier gain and scale-down factor respectively. As shown in Fig. 5, the average output current (I_{dc} (α)) is equal to the diode average current ($i_{D,OUT}$). In this figure D_1 shows the D_{OUT} duty cycle. I_{dc} (α) can be calculated by averaging D_{OUT} current over a line period as expressed in (3).

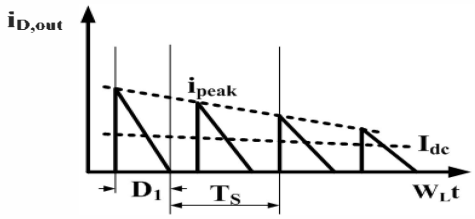


Figure 5. Diode current of D_{OUT}

$$I_{dc}(\alpha) = \frac{1}{\pi}\int_{a}^{\pi} \frac{V_p\, D(\alpha)\, T_S}{2L_e} D_1\, sin(\omega_L t) d(\omega_L t)$$
$$= \frac{V_p\, D(\alpha)\, T_S}{2\pi L_e} D_1 (1 + cos(a)) \quad (3)$$

Where V_p is the line peak voltage, D is the duty cycle, T_S is the switching period and L_e represents the parallel equivalent of the L_{PFC} and L_1. Duty cycle D_1 can be expressed as (4).

$$D_1 = \frac{V_p}{V_{dc}} D(\alpha) \quad (4)$$

Where V_{dc} is the DC-Link voltage of SEPIC converter. Therefore output power of SEPIC converter can be expressed as (5) derived from relationships (2) and (3).

$$P_{o,avg}(\alpha) = V_{dc}(\alpha) I_{dc}(\alpha) =$$
$$\left[\frac{1}{G}\left(G\, V_{dc,max} - \frac{\alpha K}{\pi}\right)\right] \frac{V_p{}^2\, D(\alpha)^2\, T_S}{2\pi L_e V_{dc}} (1 + cos(\alpha)) \quad (5)$$

SEPIC converter input power is given by (6).

$$P_{i,avg}(\alpha) = \frac{1}{\pi}\int_{a}^{\pi} V_s(\omega_L t)\, i_s(\omega_L t)\, d(\omega_L t)$$
$$= \frac{V_p I_p}{2\pi}\left((\pi - \alpha) + \frac{sin(2\alpha)}{2}\right) \quad (6)$$

Where I_P is the line input peak current. Duty cycle variations followed by firing angle changes can be expressed as (7).

$$D(\alpha) = \frac{1}{V_p}\sqrt{\frac{2P_{i,max}\; L_e V_{dc}\left((\pi-\alpha)+\frac{sin(2\alpha)}{2}\right)}{\left[\frac{1}{G}\left(G\, V_{dc,max} - \frac{\alpha K}{\pi}\right)\right](1+cos(\alpha))\, T_S}} \quad (7)$$

Equation (7) shows that increasing firing angle, reduces the duty cycle. Maximum duty cycle occurs at $\alpha=0^0$ and can be expressed as a function of maximum power as determined by (8).

$$D(0) = D(max) = \frac{1}{V_p}\sqrt{\frac{\pi\; L_e\, P_{i,max}}{T_S}} \quad (8)$$

Another formation of (5) can be expressed as (9). $\alpha=0^0$ results in maximum output power as expressed in (10).

$$P_{o,avg}(\alpha) = V_{dc}(\alpha) I_{dc}(\alpha)$$
$$= \frac{V_p\, D(\alpha)\, T_S}{2\pi L_e} D_1 \left[\frac{1}{G}\left(G\, V_{dc,max} - \frac{\alpha K}{\pi}\right)\right](1 + \cos(\alpha)) \quad (9)$$

$$P_{o,max}(0) = V_{dc}(0) I_{dc}(0) = \frac{V_p\, D(0)\; V_{dc,max} T_S}{\pi L_e} D_1 \quad (10)$$

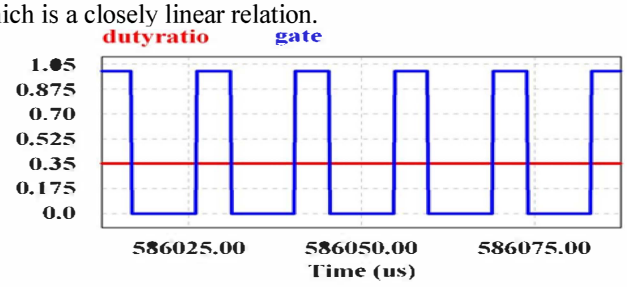
Normalized output power can be determined by (11).

$$P_{o,nor}(\alpha) = \frac{D(\alpha)}{2\, V_{dc,max}\, D(0)}\left[\frac{1}{G}\left(G\, V_{dc,max} - \frac{\alpha K}{\pi}\right)\right](1 + cos(\alpha)) \quad (11)$$

Large amount of "K", confines the firing angle variations and results in high PF even at very low output lights. Dependence of output power to the firing angle limits the use of large values for "K" in practical applications.

V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results of the proposed dimming circuit has been presented to verify the analysis, design and applicability of proposed dimming circuit. The circuit was simulated through PSIM software with a power dependent lamp model as expressed in [13]. In laboratory implementation a 42Watt CFL was used and the control circuitry was accomplished by analogue devices. Fig. 6 and Fig. 7 show the duty cycle variation in low, moderate and high power ratings for both simulation analysis and experimental implementation. Fig. 6(a) and Fig. 7(a) show that for $\alpha=0^0$ and maximum lamp power, the duty cycle would be D=0.35. In Fig. 6(b) and Fig. 7(b) at the moderate power rate $\alpha=54^0$ and D=0.26 can be seen. In the same way Fig. 6(c) and Fig. 7(c) at the low power rating of lamp show $\alpha=108^0$ and D=0.175. Fig. 8 shows the duty cycle variations by firing angle changes which is a closely linear relation.



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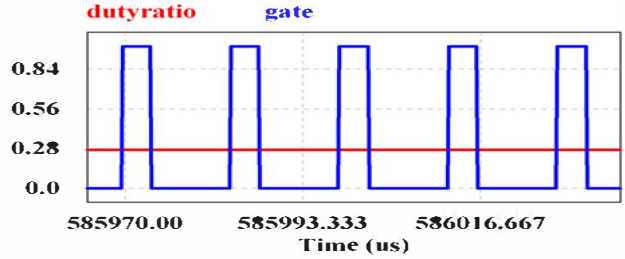

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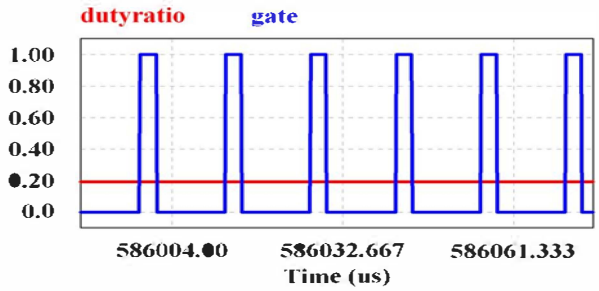
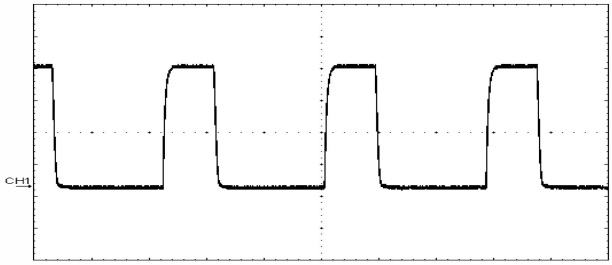


(c)

Figure 6. Duty cycle variation by firing angle; waveforms for three power levels a) $\alpha=0^0$,b) $\alpha=54^0$,c) $\alpha= 108^0$ (simulation resuls) .



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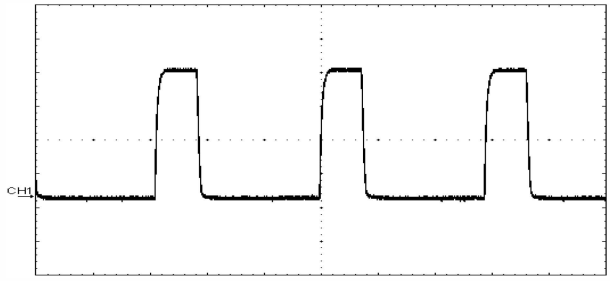

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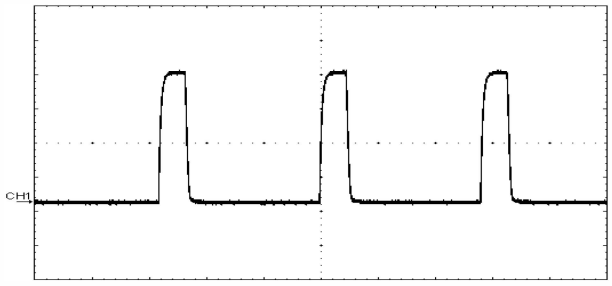


(c)

Figure 7. Experimental results, Gate pulses for different firing angles a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$(CH1:5 V/div; time:5µs/div).

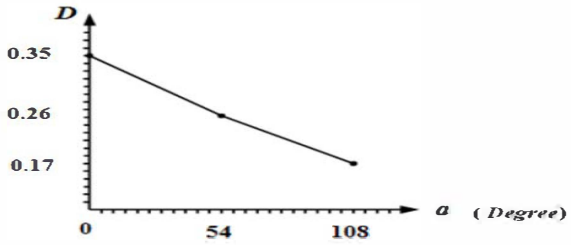


Figure 8. Linear relation between Duty cycle and firing angle.

Fig. 9 shows the simulation results of current and voltage waveforms of switch at full power condition. Fig. 10 shows the experimental results of voltage and current of the switch. Fig. 9 shows that switch peak voltages reaches to 600 V (twice the input line peak voltage). As shown in Fig. 9 and Fig. 10, there are no disturbing current and voltage peaks on the switch.

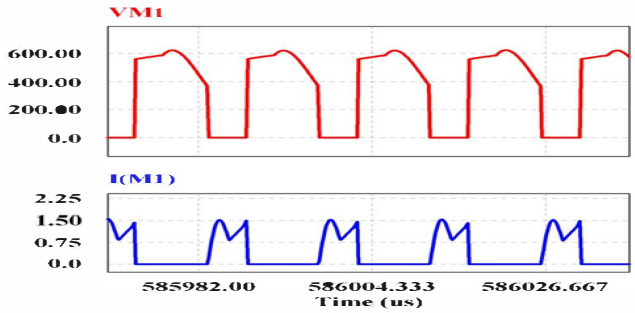


Figure 9. Simulation results for switch voltage (in volts) and current (in amperes) for $\alpha=0^0$.

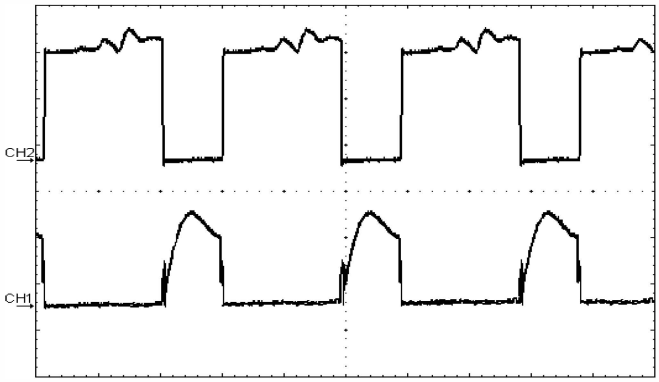
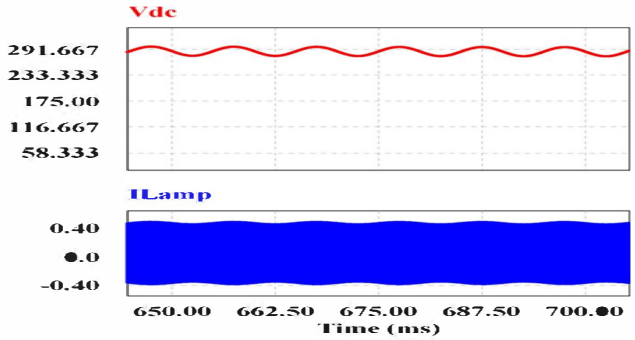


Figure 10. Experimental results for switch voltage(CH2) and current (CH1) (CH1:500 mA/div ; CH2:200 V/div; time:5µs/div).

Fig. 11 shows the DC voltage and lamp current for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$ in simulation. 20V peak to peak ripple with twice line frequency exists on the DC voltage. DC voltage would be 290V for maximum output power. When firing angle increases, lamp peak current and the DC voltage decreases which shows reduction of lamp power. In this case at low, moderate and high power ratings, the lowest value for lamp peak current would be 0.4A, 0.2A and 0.08A for $\alpha=0^0$, $\alpha=54^0$, $\alpha=108^0$ respectively.



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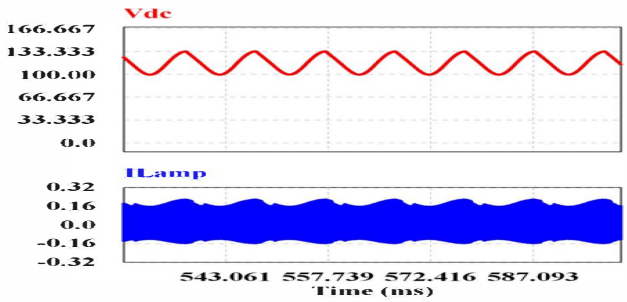

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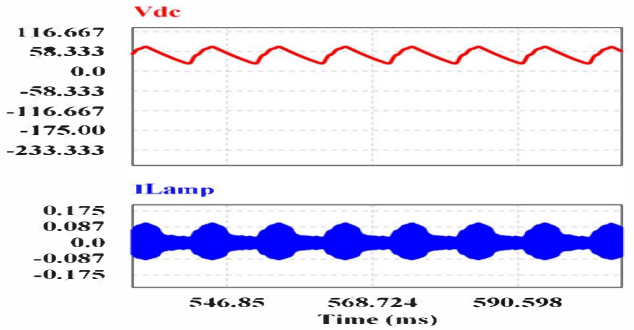
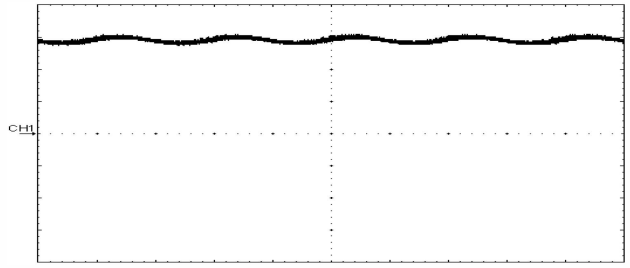


(c)

Figure 11. Simulation results for DC voltage (in volts) and lamp current (in amperes) for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$.

Fig. 12 shows the experimental results for high, moderate and low power ratings. 20V peak to peak ripple voltage shows a great compliance with simulation and analysis results.



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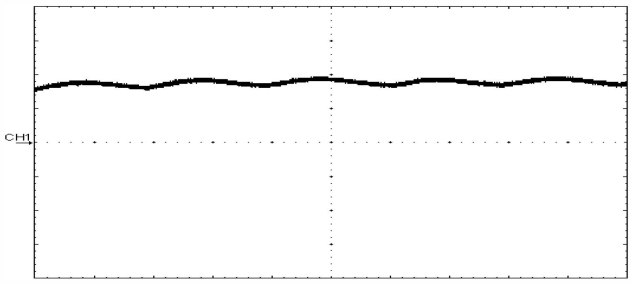

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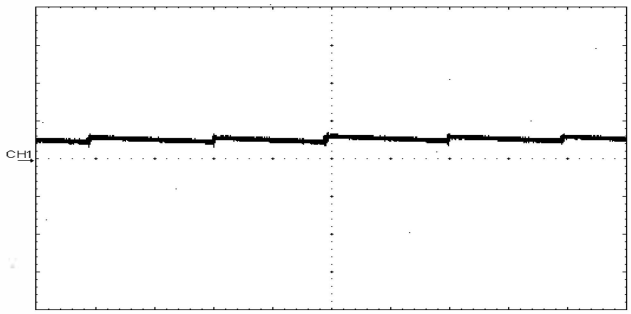
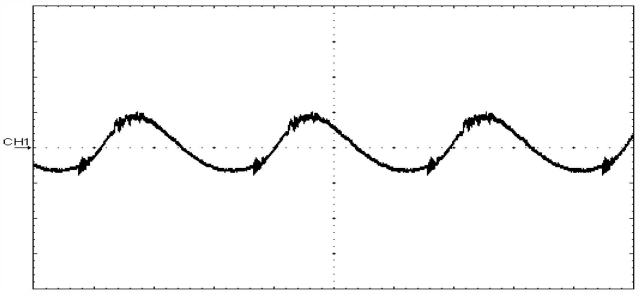


(c)

Figure 12. DC voltage experimental results for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$(CH1:100 V/div; time:5ms/div).

Lamp current in experimental implementation was measured as shown in Fig.13. Increasing firing angle, decreases lamp peak current and controls its power linearly.



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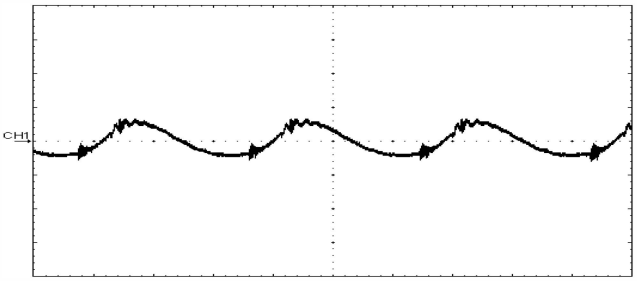

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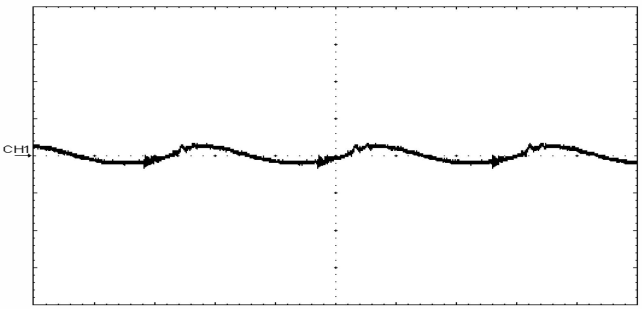
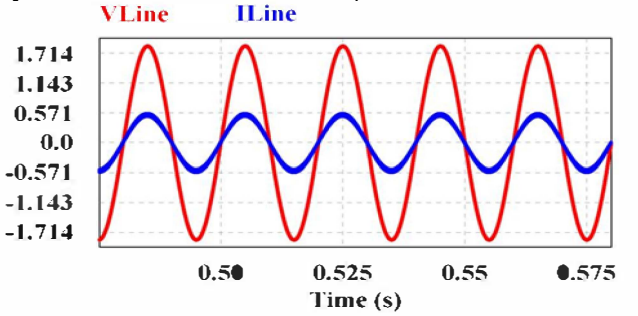


(c)

Figure 13. Lamp current experimental results for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$ (CH1:500 mA/div ; time:5µs/div).

Fig. 14 and Fig. 15 show the input voltage and current for simulation and experimental results. In order to show the voltage and current inputs in a graph, we have shown the input voltage with the ratio of 0.006 V_{in} and the input current with $2I_{line}$. In phase input voltages and input currents in various firing angle along with low harmonic content of input currents are achieved from the proposed circuit. High input PF can be easily seen in both simulation and experimental results.



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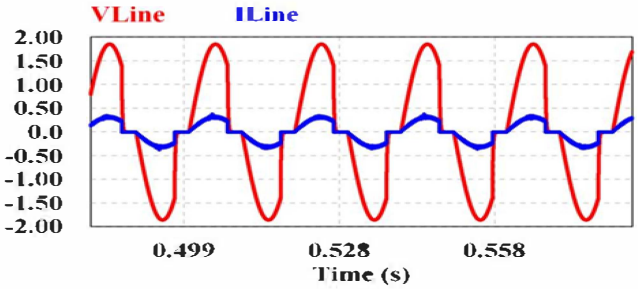

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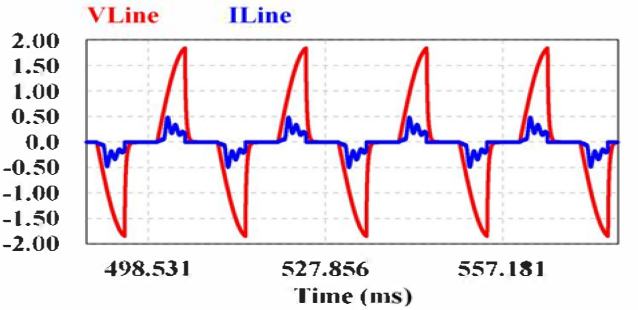

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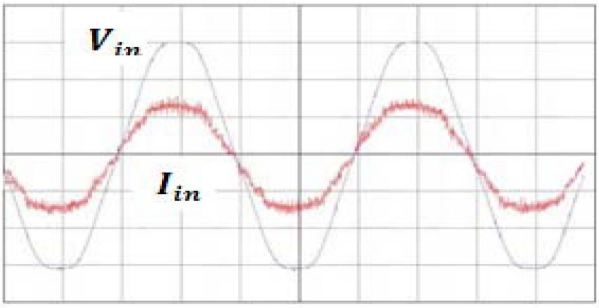
Figure 14. Input voltage (in volts) and input current (in amperes) in simulation process for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$.



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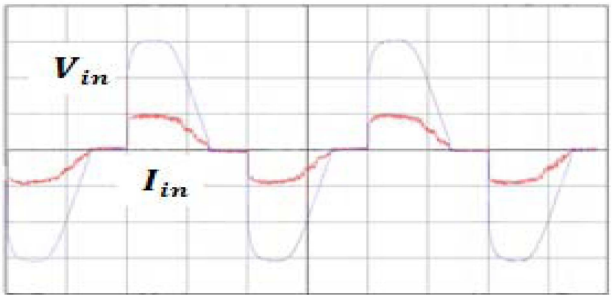
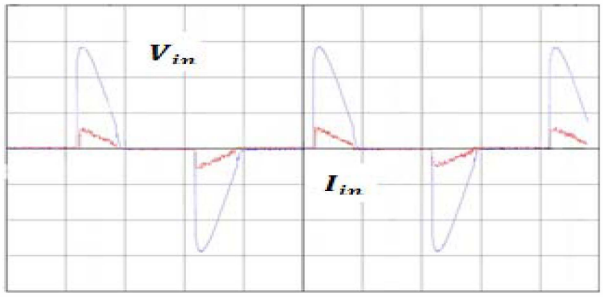


(b)



(c)

Figure 15. Input voltage and current in experimental implementation for a) $\alpha=0^0$, b) $\alpha=54^0$, c) $\alpha=108^0$ (V_{in}:100 V/div ; I_{in}:200 mA/div ; time:5ms/div).

VI. CONCLUSION

In this paper a new dimming circuit compatible with phase-cut dimmers for CFLs without the need of additional wiring is proposed. The proposed control circuitry operates by duty cycle control followed by firing angle control, this circuit is implemented by low cost analog devices and successfully tested. The proposed control circuitry is applied to the power stage of a CFL electronic ballast and tested over a wide range of light control, it achieves high input PF at the whole of firing angle range. Simulation and experimental results on the 42W CFL laboratory prototype illustrated linear light control with high input power factor. The proposed control circuit increases only 5 to 10 percent of the CFL cost depending on the CFL power (42-10W).

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